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PHASE-LOCKED OPTICAL GENERATION OF mmW/THz SIGNALS

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14. ABSTRACT
In this report, an effort to demonstrate a highly efficient millimeter-wave (mmW) modulated optical source is summarized. This is achieved using an integrated heterodyne optical phase-locked loop (OPLL) built from monolithically integrated photonic and electronic circuits (ICs). The close integration of these ICs enables low feedback latency so that relatively wide linewidth semiconductor lasers can be used. This demonstration is a key step toward realizing compact practical OPLL mmW sources incorporating data modulation. The heterodyne frequency is ultimately limited by photodetector bandwidths, and the data rate is limited by the heterodyne frequency. It will be shown that the overall performance of the heterodyne OPLL is sufficient to demonstrate the feasibility of and a direct path towards multilevel modulation at 100Gbps data rates of a mmW carrier frequency in the 100GHz to 300GHz range. This successful demonstration of the OPLL heterodyne source is a critical demonstration required to allow electronic and photonic components, now developed for advanced future fiber optic communications systems, to be directly adopted for high capacity optical feeds to enable 100Gbps wireless links.

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1. SUMMARY

In this report a new seedling effort to demonstrate a highly efficient millimeter-wave (MMW) modulated optical source is summarized. This is achieved using an integrated heterodyne optical phase-lock loop (OPLL) built from monolithically integrated photonic and electronic ICs. The close integration of these ICs enables low feedback latency so that relatively wide linewidth semiconductor lasers can be used. This demonstration is key to show a direct path to compact practical OPLL mmW source incorporating data modulation. The heterodyne frequency is ultimately limited by photodetector bandwidths and the data rate is limited by the heterodyne frequency. The overall performance of the heterodyne OPLL is sufficient to demonstrate the feasibility and a direct path towards multilevel modulation at 100Gbps data rates and at a generated mmW carrier frequency in the 100GHz to 300GHz range.

This successful demonstration of the OPLL heterodyne source is a critical demonstration required to allow electronic and photonic components, now developed for advanced future fiber optic communications systems, to be directly adopted for high capacity optical feeds to enable 100Gbps wireless links. More specifically, generation of advanced optical modulation formats now under development can then directly be converted from optical frequencies (~193THz) to mmW frequencies (100-300GHz) in a simplified antenna unit incorporating O/mmW and mmW/O conversion. In a conventional antenna optical feed technology a required optical link provides 100Gbps data transport to the antenna unit where mmW (de)modulation, digital signal conditioning and processing takes place. The now enabled architecture allows low-loss optical path extensions of the mmW wireless signal where the low transmission loss of fiber can be used to overcome the high free-space loss of mmW frequencies.

Table 1. Target and achieved OPLL performance metrics

	Target	**Achieved**
Generated Heterodyne Frequency:	10GHz – 40 GHz	2 GHz – 20 GHz
mmW modulation depth:	>90%	>90%
Phase Error Variance:	<0.01 rad^2	0.03 rad^2 in 2GHz bw
CNR	135 dB/Hz	120 dB/Hz (at 1GHz offset)
mmW-carrier data rate:	10 Gbps	<200 Mbps

Table 1 shows the target and achieved OPLL performance metrics. Peak measured heterodyne frequency was limited by available measurement equipment, not inherent OPLL capabilities. Phase noise will be improved by implementing SGDBR laser mirror stabilization, such as decoupling capacitors, and by reducing loop delay and increase loop bandwidth. The measured CNR was in these experiments limited by output power and receiver noise, and does not represent the potential of the OPLL. Finally, data rate was limited by the bandwidth of the forward biased phase modulators used for data modulation. Implementing fast QCSE modulators will meet overall data performance targets. Continued efforts will be expended to improve the OPLL performance.

2. INTRODUCTION

Optical Phase-Locked Loops (OPLLs) are versatile optical components for a wide range of applications. In optical communications, the OPLL allows synchronous coherent receivers where mixing the received signal with a high-power local-oscillator (LO) laser provides high sensitivity and out-of-band noise suppression [1]. For carrier-suppressed modulation schemes, a Costa's loop can be used [2]. In microwave photonics, an offset OPLL can form an attractive microwave single-sideband optical source [3] with the potential for endless microwave phase adjustment. This is an attractive property for implementation of a phased array microwave system. OPLLs may also find applications in free-space optical systems such as LIDAR systems where they allow coherent combination of several coherent optical sources [4], potentially to form large swept optical phase arrays.

So far, the central difficulty in realizing OPLLs using semiconductor lasers has been the strict relation between laser phase noise and feedback loop bandwidth. The wide linewidths observed in semiconductor lasers, typically in the MHz region, require sufficiently wide loop bandwidths, which are only possible with sub-ns feedback loop delays. In the past, this has been addressed by using low-linewidth external cavity lasers that allow longer feedback loop delays [5], or by construction of compact OPLLs using miniaturized bulk optical components to meet the delay restrictions of standard semiconductor lasers [3], [6]. Other efforts include relaxing this restriction by combining an optical phase-lock loop with optical injection locking, thereby gaining the wide locking bandwidth of optical injection, while a slow, long delay phase-lock loop allows long-term stability [7].

One particular application for OPLL's is for efficient generation of mmW/THz modulated optical carriers through stabilized optical heterodyning for application in mmW/THz wireless communications systems. Generally, wireless data rates are trailing the capacity of wired links. Currently, the 60 GHz band is developed to support data rates in the GHz region. To support up to 100Gbps wireless transmission, the high mmW band (100GHz+) must be utilized. Current electronics technology is well-set to make a contribution for these systems. High speed Silicon CMOS is on the way to reach sufficient speed to process 100Gbps channels (e.g. 4x25Gbps). Indium Phosphide electronics is currently sufficiently fast for 300 GHz RF transistors with gain. However, there exist an opportunity for photonics in these applications in performing tasks at speeds higher than can be done using Silicon, or with greater complexity, wider bandwidth and higher efficiency than Indium Phosphide electronics.

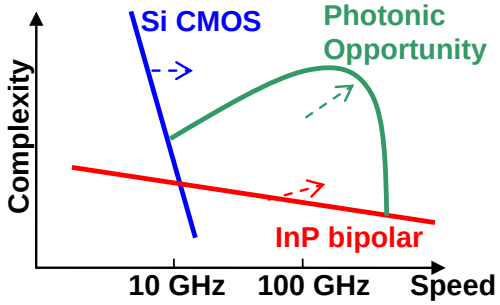


Figure 1. Schematic illustration of potential role of photonic IC's in relation to current electronics capabilities and trends.

Due to the large throughput data rate, ***optical feeds for 100Gbps antenna front-ends are required,*** coaxial transmission of this information content is not practical even over moderate distances. Current commercial optical communication technology is rapidly moving towards higher channel rates (4x25Gbps/channel) and more spectrally confined optical WDM channels to meet increasing bandwidth demands. It is expected that this technology development can be leveraged and extended to form a viable infrastructure for these high-capacity wireless links, where the optical and wireless transmission medium is utilized fully.

More specifically, digital signal processing is increasingly being researched to combat severe dispersion effects in optical fiber in a very refined manner, and at high clock rates. Although the commercial main interest is for fiber optic network backbone applications, there is no reason why this technology, once developed, cannot benefit high capacity wireless links as well. The optical link and antenna unit, including any optical analog signal processing can then be viewed as an extension of the radio path. Digital pre-processing can now be used to adaptively deliver whatever stimulus to the InP driver circuit required for error-free delivery of data to the end user. Similarly, digital post-processing can compensate for any distortion of the signal in the uplink. These processing algorithms can be similar to those developed for the various flavors of distortion affecting fiber links. The hardware of the optical link, antenna unit and user mobile station can now be optimized for size, weight and power. The alternative, using signal regeneration at the antenna unit will break up the analog link in two parts and lead to both a more complex link architecture and antenna units.

UCSB is well positioned to develop these photonic antenna feed technologies. Prof. Coldren's group has a long track record of photodetectors [8,9] and high-performance integrated photonics for generation of optical modulation [10,11]. This needs to be adopted for the spectrally well-defined multilevel waveforms required for wireless transmission. UCSB has further pioneered direct-to-baseband all-optical demodulation of multilevel modulated microwave signals [12], a technique directly applicable to demodulation of mmW signals. Prof. Mark Rodwell has been a pioneer in the development of the high mmW InP transistors required for the antenna front-ends [13].

The one remaining key technology required before development of the full system can be initiated with a high degree of confidence, is a n efficient and stable method for optical conversion of baseband signals to mmW. Optical modulators above 100 GHz are very challenging and inefficient. The generated optical signal also typically suffers from periodic fading due to fiber dispersion. Methods relying on optical multiplication, in which a harmonic RF signal is multiplied to generate the desired optical mmW modulation, are inefficient, as only two of many generated optical comb-lines are used to produce a beat note. This is very efficient, as nearly all laser power contributes to the generated mmW signal. Optical modulation on one of the laser outputs will directly be translated to mmW modulation, allowing us to take advantage of existing optical modulator technologies that can be monolithically integrated to the optical source. Optical phase-lock loop techniques will be used to correlate the laser phase noise to generate spectrally pure mmW signals. This is a more stable technique (i.e. larger hold range) than the more commonly used optical injection locking. It is also ultimately less complex. The traditional challenge for optical phase-lock loops has been a tradeoff between latency and laser

linewidth. However, we have recently demonstrated monolithically integrated structures that have the required latency to control even wide linewidth semiconductor lasers [14].

In this seedling, we demonstrate for the first time, an OPLL photonic integrated circuit (OPLL-PIC) in which all required optical components are monolithically integrated, including: lasers, passive optical waveguides, multimode interference (MMI) couplers/splitters, high-speed photodetectors, and high-speed optical phase modulators. This eliminates latencies and instabilities associated with free-space or fiber optical paths to allow very fast and robust optical phase locking. Moreover, in our case, the OPLL-PIC uses widely-tunable Sampled Grating Distributed Feedback (SG-DBR) lasers that have a wavelength tuning range greater than 5 THz. This is a key feature as together with a THz photodetector and electronics, it will allow optical heterodyne signal generation with a DC to 5 THz frequency range with maintained coherence. Applying optical phase or amplitude modulation to one optical line can be used to generate a coherent phase or amplitude modulated THz signal.

Table 2 shows tasks and schedule for the program. In the following, details of the work and outcome of the five tasks are summarized.

Table 2. Schedule

Task	3 mo.	11 mo.	Cost
1. System Analysis and modeling	Complete analysis of full system. Provide flow-down performance req. for components (3 mo.)		$50k
2. Design of PICs	Design/fab photomask and PIC layer structure. (3 mo.)		$50k
3. Design of EICs	EIC designs for qualified foundry fabrication (3 mo.)		$50k
4. PIC fabrication		Complete fab of PICs. Thin, cleave, AR coat, mount, pre-test PICs (8 mo.)	$140k
5. System demonstration		Full characterization of (EIC+PIC) integrated OPLL mmW source (11 mo.)	$90k
Total			$380k

3. TASK 1 - ANALYSIS AND MODELING

Task description *- Perform analysis of the full optical mmW remoting system. Not only incorporate the optical phase-lock loop mmW generation technology which is the focus for this seedling, but also the larger system to which the OPLL relates to. Evaluate different architectures for optical mmW feeds in terms of complexity, performance and component requirements. Generate flow-down performance requirements for the OPLL, as well as for optical modulators, optical-to-mmW interfaces and additional and optional optical processing functions such as demodulation in the optical domain.*

In more detail; analyze optical phase-lock loop architectures. Generate models including detector impulse response, feedback amplifier impulse response and laser current tuning response. Determine required feedback filter response for stable OPLL operation. From model, estimate OPLL performance, including laser phase noise suppression and dynamic effects including lock-up time.

3.1. OPLL Basics

An OPLL has both parallels and fundamental differences when compared to its RF equivalents. In a microwave loop, it is a voltage-controlled oscillator that typically tracks the input. In an OPLL, wavelength tuning of a laser takes this role, achieved typically by current injection [4]. An RF phase-locked loop (PLL) can be built using spectrally pure oscillators, which allow stable operation in a narrowband loop to enable filtering, or it can be built using compact integrated circuits to have a substantial fractional loop bandwidth compared to the carrier frequency, allowing agile tracking of a frequency modulated signal. In contrast, an OPLL is constructed using less compact optical components, leading to a smaller loop bandwidth, and with a carrier frequency of ~193THz (1550nm), which results in low loop bandwidth to carrier frequency ratio. As a result, acquiring locking is less straightforward in an OPLL as the slave laser must be tuned to the master laser wavelength with high accuracy.

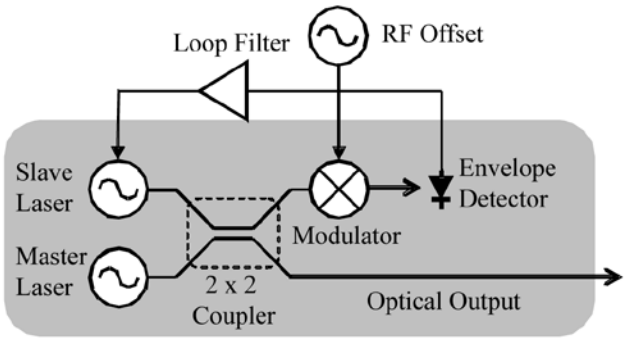


Figure 2. Schematic of an OPLL heterodyne offset locking experiment.

Figure 2 shows a simple schematic of the OPLL architecture demonstrated in this work. Two widely tunable SG-DBR lasers are monolithically integrated on a single InP substrate along with all of the other optical components needed to form the OPLL. One laser takes the role of a master laser, while the other takes the role of a slave laser. The outputs of the two lasers are first combined using a 2x2 optical coupler. The combined beat signal is then amplitude modulated for offset-locking using an integrated optical modulator and envelope- detected using an integrated photodetector. After balanced photodetection, the detected RF signal can be written:

$$i_s = 2R\sqrt{I_m I_s}\cos[(\omega_m - \omega_s)t + \phi_m - \phi_s] \quad (1)$$

Where I, ω and φ are master and slave laser intensity, optical frequency and phase, respectively. After electrical mixing with the mmW reference, the current fed to the slave laser is:

$$i_c = k_{lf}k_m k_a k_{pd}\sin[(\omega_r - \omega_m + \omega_s)t + \phi_r - \phi_m + \phi_s] * h_a * h_m * h_{lf} * \delta(t - \tau_d) \quad (2)$$

Where k_{lf}, k_m,k_a and k_{pd} is the conversion gain of loop filter, mixer, amplifier and photodetector, h_{lf}, h_a and h_m are the corresponding the impulse responses, and the last term accounts for the feedback delay. When the loop is phase-locked, there will be no frequency error and only a small phase error (φ_e), so that this can be approximated as:

$$i_c = k_{lf}k_m k_a k_{pd}\phi_e * h_{lf} * \delta(t - \tau_d) \quad (3)$$

The current tuning of the laser is given by:

$$\frac{d\phi_s}{dt} = 2\pi k_s i_c * h_s \quad (4)$$

This gives us the master time-domain PLL equation:

$$\frac{d\phi_{ms}}{dt} = 2\pi K\phi_e * h_{lf} * h_s * \delta(t - \tau_d) \quad (5)$$

K is the combined gain of the loop components. Taking the Laplace transform of this:

$$\mathcal{L}\{2\pi K\phi_e * h_{lf} * h_s * \delta(t - \tau_d)\} = K\Phi_e(s)F(s)H_s e^{-s\tau_d} \quad (6)$$

The standard closed-loop (H) and open-loop (G) transfer functions can now be given as:

$$H(s) = \frac{KF(s)H_s e^{-s\tau d}}{s + KF(s)H_s e^{-s\tau_d}} \qquad G(s) = \frac{H(s)}{1 - H(s)} = \frac{KF(s)H_s e^{-s\tau_d}}{s} \quad (7a,b)$$

Given a desired second order loop transfer function: $G(j2\pi f) = -(f_{loop}f_{zero}/f^2)(1 + jf/f_{zero})$, the loop filter response, $F(s)$, must be adapted to compensate for the frequency response of the slave laser tuning section, $H_s(s)$.

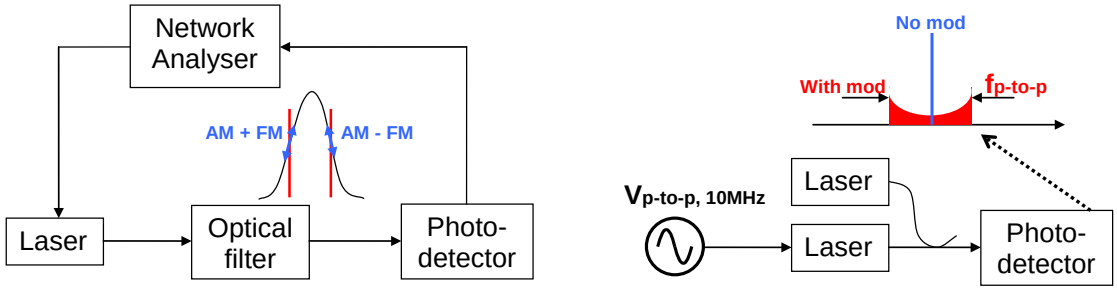


Figure 3. Left: experimental arrangement for measurement of laser FM response. Right: Calibration of absolute FM response at 10MHz.

During these three first months, new measurements of the slave laser FM response have been performed, extending the frequency range of the data. Figure 2 shows a schematic of the measurement setup used for this characterization. In this measurement, the FM response is converted to intensity modulation by tuning the center emission frequency of the laser under test to the 3-dB point of the edge of an optical filter. A frequency shift is now translated into a change in optical intensity. Residual intensity modulation from the laser can be eliminated by comparing the response from positive and negative slope at the same detected photocurrent.

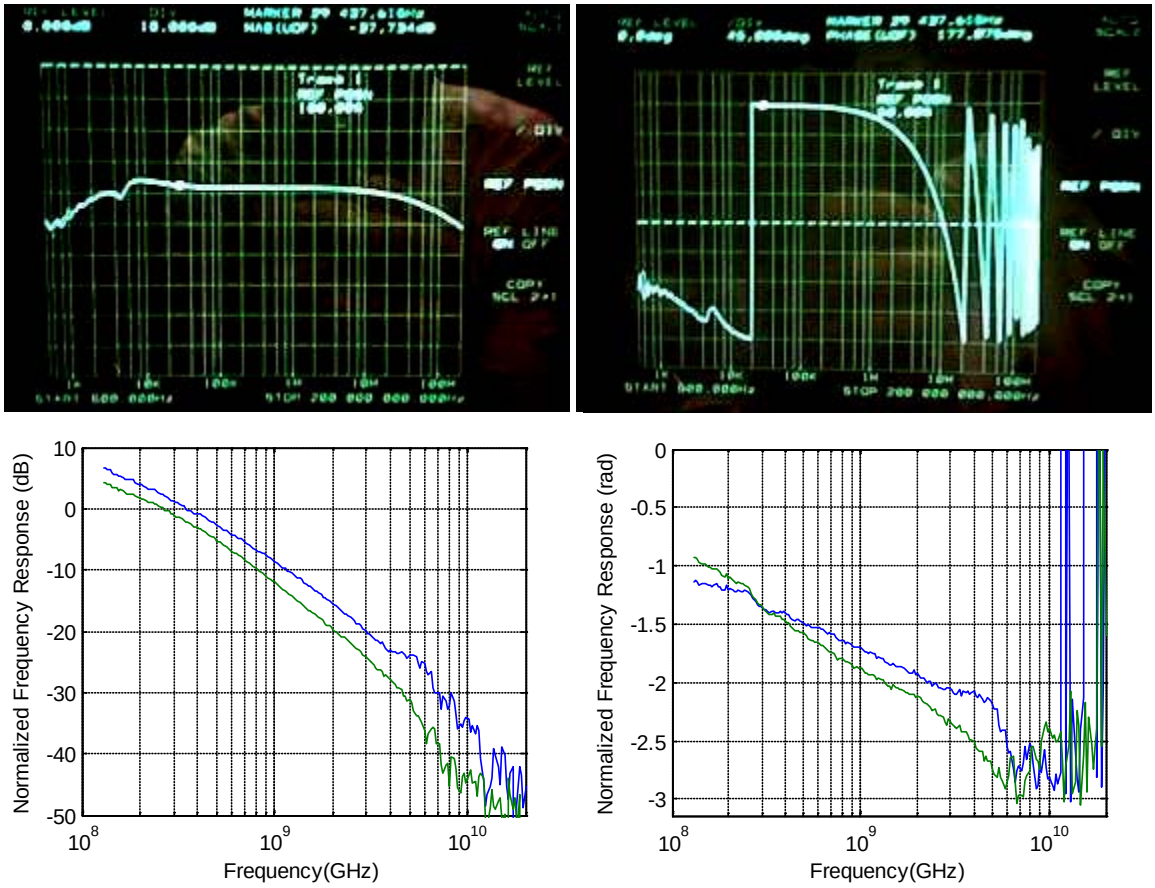


Figure 4 a-d. FM response of an SGDBR laser. Amplitude and phase of response (left, right).

Figure 4a-d shows the results of the FM response measurements from the kHz region to >10 GHz. Figures 4a and 4b show the amplitude and phase response from <1kHz to 200MHz. At lower frequencies, the roll-off of the bias-tee is clearly observed. All in all, the figures confirm that there is no phase inversion at low frequency for phase section modulation in SG-DBR lasers, the small heating effect from carrier injection in to the laser phase section is more than compensated for by the blue-shift in the response. Additionally, the FM response has a clear pole at ~70MHz frequency, after which the FM response takes on a $1/f$ type of response. At high frequencies, several GHz, an additional pole is evident in Figures 4c and 4d, gradually leading to a $1/f^2$ response around 10GHz. This pole originates from parasitic capacitances in the laser phase sections, where no passivation etch was performed and a low-frequency pad layout was used.

Figure 5 shows the calibrated FM magnitude at 10 MHz as a function of phase section bias current. This absolute FM calibration is obtained by observing the laser line-broadening under frequency modulation. This was performed at a fixed frequency of 10MHz.

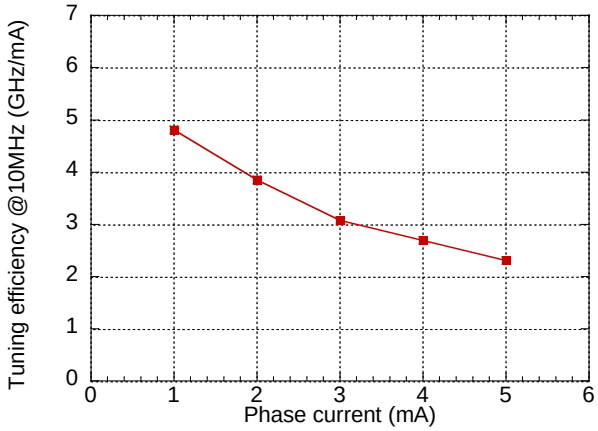


Figure 5. Magnitude of laser FM response at 10 MHz as a function of phase section bias.

Given the measured FM response, a loop filter design taking this into account can now be calculated. The result is shown in Figure 6. The redesigned filter now compensates both the pole in the FM response as well as providing the required lag compensation zero.

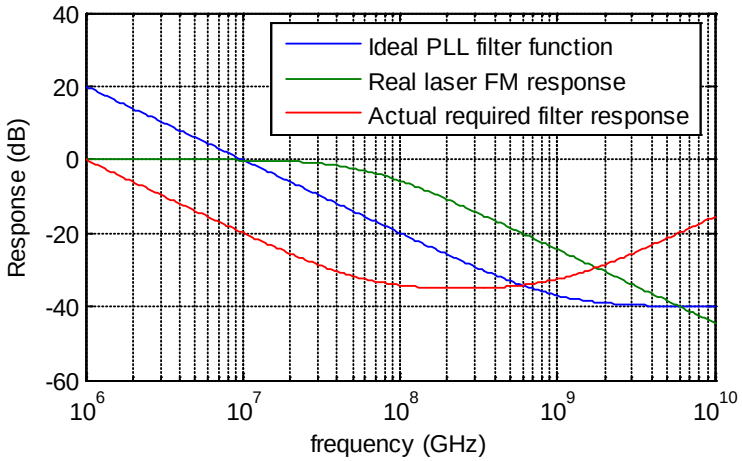


Figure 6. Ideal and corrected OPLL loop responses. Uncalibrated magnitudes.

The full simulated PLL loop response can now be calculated. Based on Photonic and electronic IC designs outlined below, the estimated loop delay is ~100ps. This is around three times greater than the recent PHOR-FRONT PLL's developed at UCSB. The extra delay originates from a more relaxed photonic IC design combined with a modular electronics approach. Assuming 5 mA average photocurrent per detector, 10dB mixer conversion loss, the measured FM response and 100ps loop latency, the calculated required loop filter response, the real open-loop gain function can be plotted, as shown in Figure 7, below. As can be observed, a loop natural frequency of 1GHz is well supported, with adequate margin for stability (10dB gain margin and 60deg phase margin).

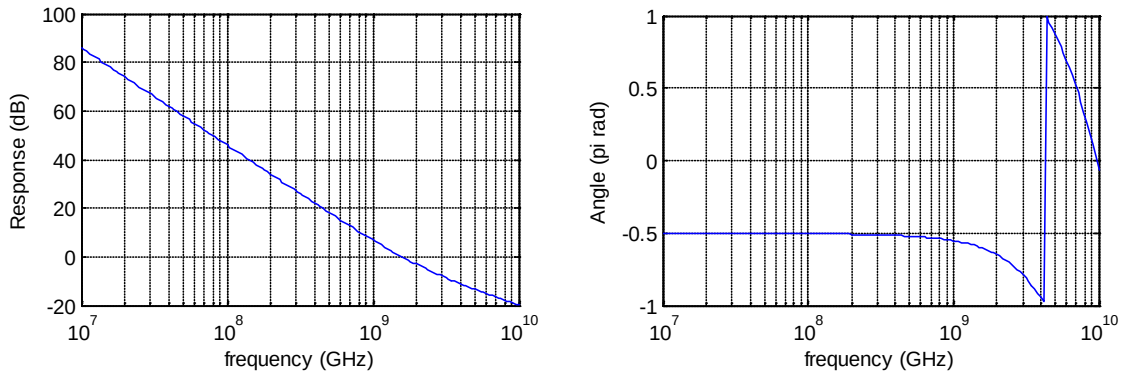


Figure 7. Magnitude (left) and phase (right) of calculated open loop gain function.

Given that the available loop natural frequency is known, the loop tracking performance can now be estimated. For a second order loop, such as this, there are known expression for loop tracking. Assuming unity damping factor, the transient phase error from a frequency step is given by:

$$\theta_e = \Delta\omega t \cdot \exp(-\omega_n t) \tag{8}$$

Where $\Delta\omega$ is the frequency step and ω_n is the loop natural angular frequency. Similarly, the phase error due to a frequency ramp is given by:

$$\theta_e = \frac{\Gamma}{\omega_n^2}(1-\omega_n t)\exp(-\omega_n t) \tag{9}$$

Where Γ is the frequency sweep rate (rad/s/s). Figure 8 plots the predicted tracking capability of the OPLL. The left plot show the transient response for a frequency step. It is seen that the possible frequency step is proportional to the loop bandwidth. For 1 and 2 GHz, the peak phase error is <1 rad and the loop will not cycle-slip. The phase error will reach zero after a few ns. The right plot shows the response for a frequency ramp. Unlike for a frequency step, a second order loop will result in a static phase error with a ramp. The maximum frequency ramp a second order loop can track is proportional to the square of the loop bandwidth and given by Γ/ω_n^2. A 1GHz loop can track a frequency sweep rate up to 1GHz/ns.

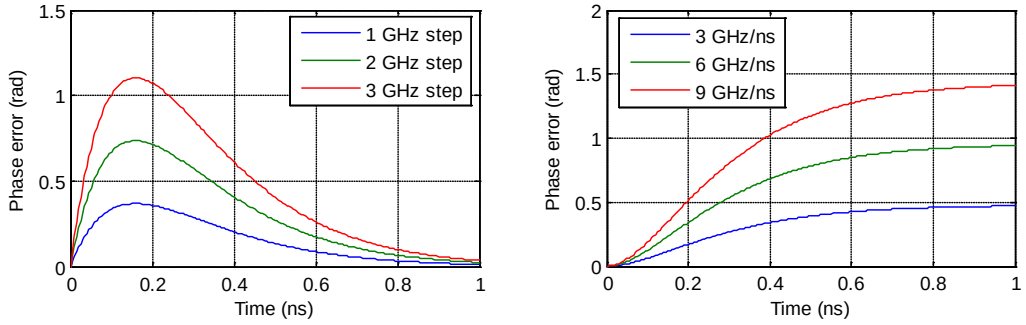


Figure 8. Loop response to frequency step (left) and frequency ramp (right).

4. TASK 2 – PIC DESIGN

***Task Description**: Based on initial modeling, design different integrated OPLL PICs, including dual-laser chips for offset phase-locking, initially in the mm-wave region, but in the extension applicable to THz frequencies. Additionally, design single-laser chips for locking to an external optical reference for receiver applications or optical frequency synthesis. Lay out photo-mask patterns and review. Include on-chip diagnostic patterns to verify fabrication as well as operation of PIC. Complete mask sets and review.*

Figure 9 (a) and (b) show schematics of our two different OPLL-PIC designs. The design shown in Fig. 2(a) is intended for locking of an on-chip tunable laser to an external laser, while the design shown in Figure 9 (b) is intended for offset locking of two on-chip tunable lasers. Each OPLL-PIC design comprises of three sections that are labeled in Figure 9 (a) and (b) as: Laser Section, Middle Section, and Output Section. We choose the SG-DBR laser because of its wide tuning range, large frequency-modulation (FM) tuning sensitivity, and absence of phase inversion in the frequency response, as explained in Section III.

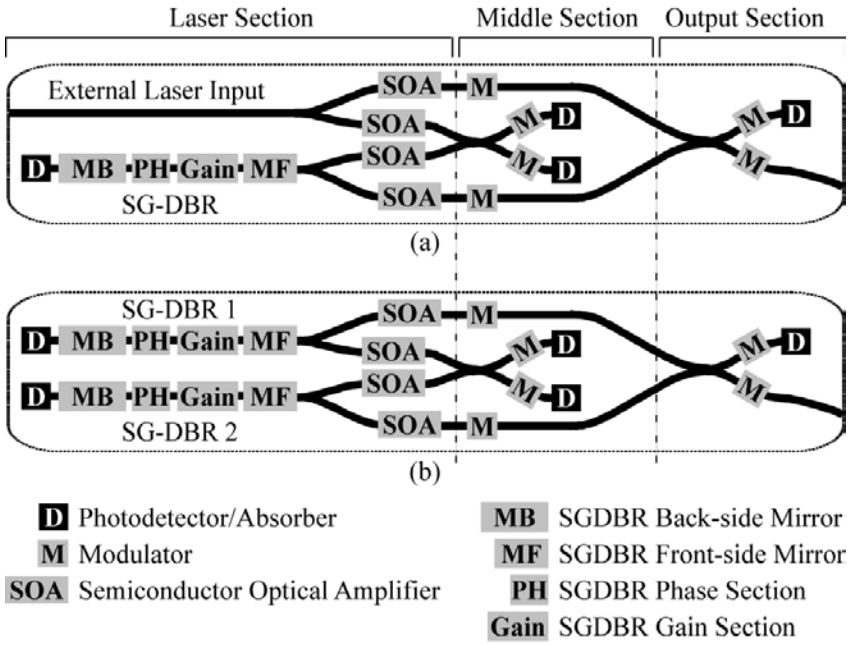


Figure 9. Schematic of (a) an OPLL-PIC for locking to an external laser and (b) an OPLL-PIC for offset locking of two on-chip lasers.

In Figure 9(a) and (b), we explicitly show the constituent components of the SG-DBR laser: front-side mirror (MF), gain section, phase section (PH), back-side mirror (MB), and back-side absorber/photodetector (D). Light from each laser is first split using 1×2 MMIs into two half-power components. One of the two half-power components from each laser is directed into a 2×2 MMI, which is a part of the feedback loop, and which is located in the Middle Section of the OPLL-PIC. The remaining half-power component from each laser is directed into a 2×2 MMI in the Output Section of the OPLL-PIC. Each of the four half-power optical paths has a semiconductor optical amplifier (SOA) to adjust the optical power in each path. Each optical path at the output of the 2×2 MMI coupler in the middle section of the OPLL-PIC contains a

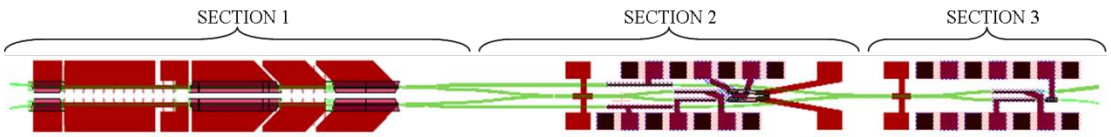
phase modulator (M), followed by a photodetector (D), which can be used in a balanced receiver configuration. Similarly, each optical path at the two outputs of the 2×2 MMI in the Output Section of the OPLL-PIC contains a phase modulator. One of these two output waveguides ends upon a photodetector that can be used for electrical-domain monitoring of the interference resulting from the beating of the two lasers. The other output waveguide extends to the edge of the OPLL-PIC to enable coupling into an optical fiber and can be used for optical-domain beat monitoring. The 2x2 MMI in the Output Section has phase modulators on its input waveguides as well, which can be used for additional phase control.

4.1. Mask Design:

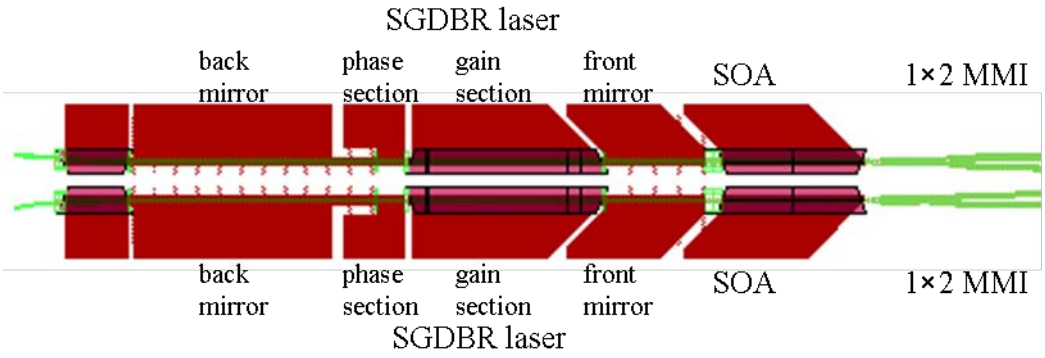
As also shown in the project proposal, Figure 9 illustrates the schematics of our PIC, not including the feedback EIC connected to the phase section of one of the two SGDBR lasers, controlling its phase/frequency. We included several variations of the PIC on the actual mask, one of which is shown in. In Figure 10, this PIC variation is shown in its entirety, and, consequently, the constituent components of the PIC are not clearly visible. The length of the PIC is about 6.7 mm, while the width is about 0.46 mm (largely determined by the p-metal contact pad shown in red). For the purpose of clearer presentation, the device is thus divided into three sections, SECTION 1, 2, and 3 [as shown in Figure 10(a)], which are enlarged in Figure 10 (b)-(d), respectively.

As shown in Figure 10(b) (SECTION 1), the PIC starts with two identical SGDBR lasers, commonly used in Prof. Coldren's group at UCSB. Each lasers is about 2 mm long, and it is followed by a 400 µm long SOA. Placement of the SOAs in the PIC is one of the variations that has been introduced in the mask. Following each SOA is a 1×2 MMI. The green layer that appears to be optical waveguide is actually the typical Proton Implant/Isolation Etch layer used for optical loss reduction, which is about 13 µm wide, and which surrounds a 3-µm-wide surface-ridge optical waveguide, not visible in the figure. This very combination of SGDBR, SOA, and 1×2 MMI, based on 3-µm surface-ridge waveguide, has been optimized in previous projects in Prof. Coldren's group. Also, based on the group's experience, the separation between the two lasers is made large enough (about 100 µm) to avoid thermal coupling issues, while being small enough to avoid excessive optical loss in curved waveguide sections. The purple regions in the SGDBR lasers and SOAs are wet-etch-defined gain sections, also referred to as "active" regions in the fabrication discussion bellow. The fabrication discussion will also address the grating bursts in the front and the back mirrors of the SGDBR laser.

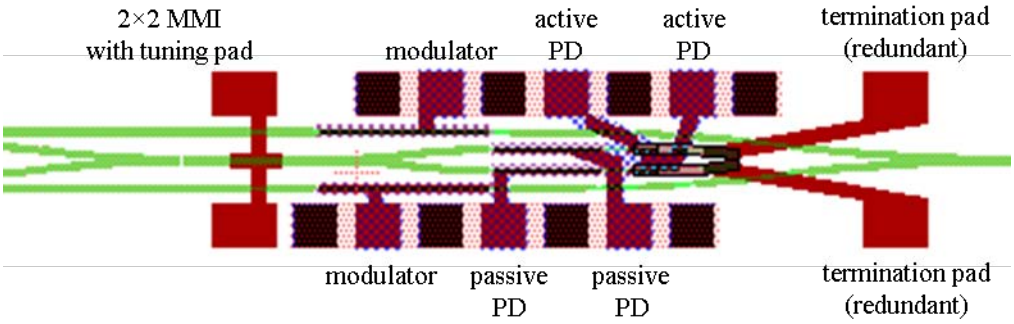
Figure 10(c) illustrates the middle section of the PIC (SECTION 2). The section starts with a 2×2 MMI needed to combine half of the lasers' output in a balanced detector, while the other half of the lasers' output is combined in the output 2×2 MMI, partly shown at the end of SECTION 2 and at the beginning of SECTION 3, and this light represents the optical output of the PIC. The MMIs have tuning pads that can be used to fine-tune the splitting ratios between their output waveguides to be as close to 50% / 50% as possible.



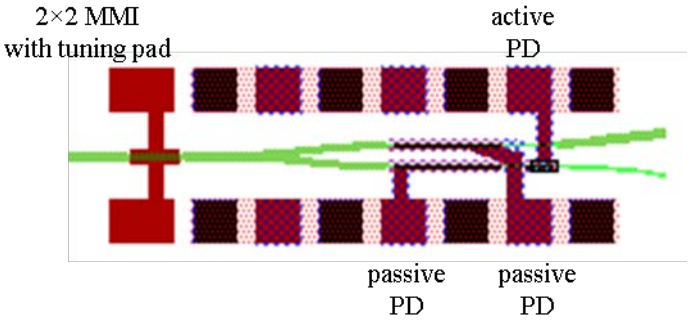
(a)



(b)



(c)



(d)

Figure 10. One of several mask variations of the PIC. (a) the entire PIC divided into SECTION 1, 2, and 3 for clearer presentation, (b) SECTION 1, (c) SECTION 2, and (d) SECTION 3.

As Figure 10(c) further shows, there are two 400-µm-long modulators that can be used to modulate the output millimeter-wave beat. Unlike the active sections that contain quantum wells with the lowest-energy gain/absorption peak (corresponding to forward/reverse bias) at the

wavelength close to 1.550 µm, the modulators are termed passive because they consist of bulk material having band edge at 1.400 µm (1.4Q material), which does not provide considerable absorption for wavelengths close to 1.550 µm. The core of the optical waveguide is the same 1.4Q material, so that the modulation is practically achieved by applying voltage bias to the optical waveguide. Positive bias will produce the current-injection-based modulation, while the negative bias will modulate the propagating light via the Franz-Keldysh effect. Similar to the photodetectors used in the PIC, the modulators have BCB underneath the P-side metal, for low capacitance and high-frequency operation, while they share a common ground as the bottom of the InP wafer is Si-doped. The fast modulators and photodetectors are connected to G-S-G-S-G-S-G pads, which can easily be access with in-line RF probes. The G (ground) pads provide top-side access to the ground for the fast modulators and detectors. Other, slow devices, access the ground via a back-side metalized contact.

The balanced detector can be obtained by making an off-chip connection between two 250-µm-long passive photodetectors, or two 50-µm-long active photodetectors that also absorb most of the incident light and thus prevent undesirable reflections. The termination pads that are also shown in Figure 2(c) can be used to detect/collect photocurrent generated at this optical termination.

Lastly, Figure 10(d) (SECTION 4) shows how the PIC's output light can be collected from the top branch of the output 2×2 MMI, as it does not contain the active photodetector which absorbs most of the light. The active detector, or either of the two passive detectors can be used for on-chip detection of the millimeter-wave beat. The output waveguide is widened and curved in order to minimize undesirable optical reflections. In addition, for the same purpose, the sample will be AR coated.

Besides numerous test structures, the mask contains twelve PICs that have six different variations. For example, in some cases two additional SOAs have been added, or one of the SGDBR lasers have been omitted and replaced with an input waveguide, so that the other SGDBR laser can be phase-locked to an external source. Figure 11 illustrates two of these variations.

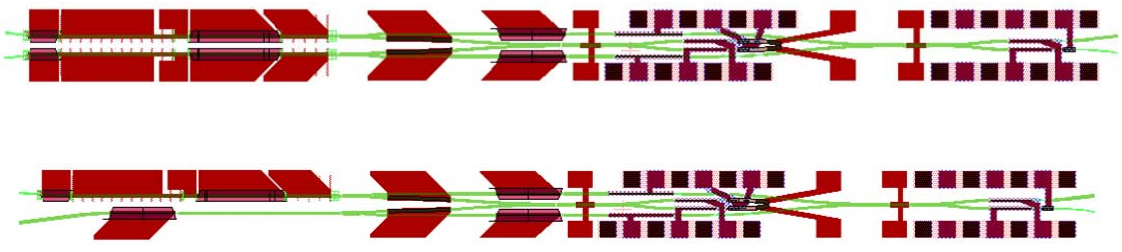


Figure 11. Two examples of PIC variations on the mask: (a) addition of two SOA and (b) removal of one of the two SGDBR laser for phase-locking to an external source.

5. TASK 4: OPLL-PIC FABRICATION

***Task Description**: Once layer structures are decided, develop MOCVD growth procedures to create desired PIC wafers. Grow wafers. Develop fabrication plan for patterning wafers using photo-mask set. Refine fabrication procedures to insure that various fabrication steps will work. Fabricate PICs—use test patterns to verify that each fabrication step is proceeding properly. Wafer probe to insure some level of functionality. Thin wafers for cleaving. Cleave & AR coat chips.*

5.1.Process design

For monolithic integration of the SG-DBR lasers with the other components of the OPLL-PIC, we use an integration platform that is often referred to as "Offset Quantum Well (OQW)" Platform [15]. In this platform, the light is guided by a "passive" 1.4Q bulk layer that forms a basis for waveguiding, as well as modulation through current injection or the Franz-Keldysh effect if reverse biased. Above this layer, light couples evanescently to an "active" multiple-quantum-well (MQW) layered structure that is present only in the regions that form SOAs, gain sections of SG-DBR lasers, and photodetectors.

	150 nm InP, Zn (1e18 cm^{-3})
	60 nm InP, UID
	30 nm 1.2Q, UID
"active layer"	119 nm MQW, UID
	10 nm InP, UID
	20 nm 1.2Q, UID
"passive layer"	300 nm 1.4Q
	2000 nm InP, graded Si-doped
	S-doped InP substrate

Figure 12. "Offset Quantum Well" base epitaxial structure.

Figure 12 shows details of the base epitaxial layer structure used in the OQW platform that is grown on a 2-inch S-doped InP wafer by Metal-Organic Chemical Vapor Deposition (MOCVD). A 2 µm thick Si-graded-doped InP buffer is grown on the substrate to reduce the overlap of the optical mode confined to the 1.4Q waveguiding layer with the heavily doped substrate and minimize the free-carrier-induced optical propagation loss in the waveguide. The buffer doping is graded from ~1e19 cm^{-3}, close to the substrate, to ~1e18 cm^{-3}, close to the 1.4Q waveguide core layer. A 300 nm thick, unintentionally doped (UID), 1.4Q waveguiding layer is epitaxially grown over the graded InP buffer, followed by a 20 nm thick 1.2Q separate confinement heterostructure (SCH) layer, a 10 nm thick InP etch-stop layer, an active region comprised of Multiple Quantum Wells (MQW) layers with a total thickness of 119 nm, another 30 nm thick 1.2Q SCH layer, a 60 nm thick UID InP spacer, and a 150 nm thick Zn-doped (1e18 cm^{-3}) InP cap. The thin InP spacer underneath the Zn-doped InP cap helps prevent diffusion of Zn dopant into the active MQW layer, and the Zn doping in the InP cap helps in controlling the position of the p-i-n junction formed after regrowth. The Photoluminescence peak of the active MQW layers was measured to be ~1560 nm.

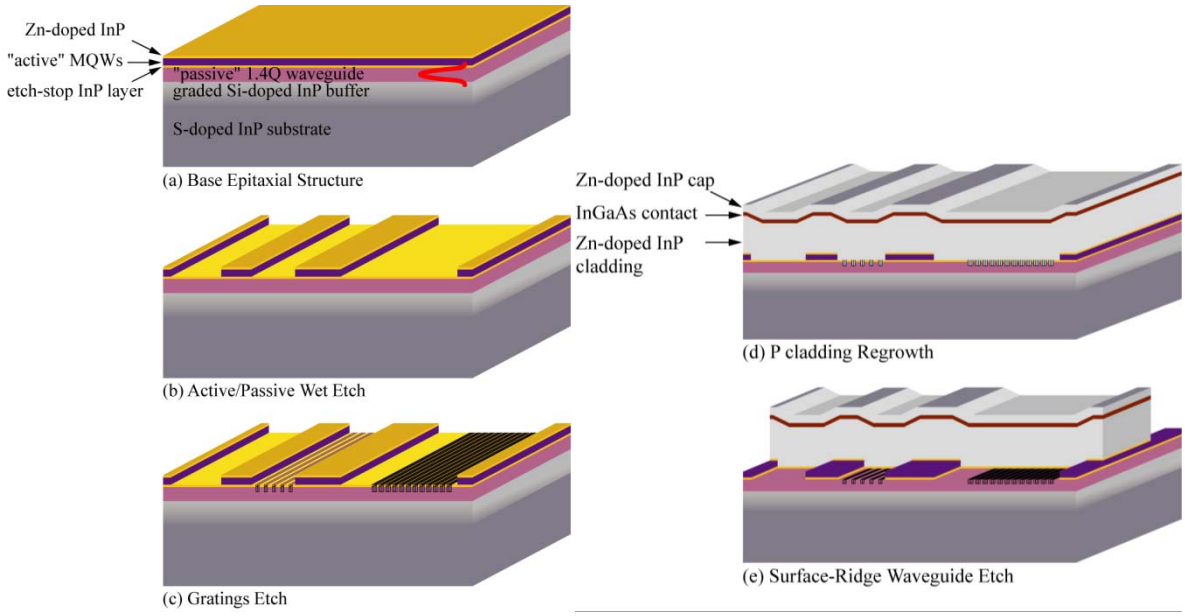


Figure 13. "Offset Quantum Well Platform": schematics of the main processing steps starting with the base epitaxial structure.

Figure 13. 5(a)-(e), we illustrate the processing steps used in the fabrication of the OPLL-PIC. Starting from the base epitaxial structure shown again in Figure 13(a),(b) illustrates the active/passive wet etch step, where the "active" regions are etched away everywhere on the wafer except in the areas that define the SOAs, gain sections of the SG-DBR lasers and the photodetectors. A 100 nm thick Silicon Nitride (SiN_x) layer is deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD), and 5× Stepper Lithography is used to define the active regions by patterning photoresist that is spun on top of the SiN_x layer. The pattern is transferred to SiN_x by CF_4/O_2-based Reactive Ion Etching (RIE). The SiN_x hard mask protects the InP cap, spacer layers at the top of the wafer, and the active MQW and SCH regions during wet etching steps that selectively remove these layers elsewhere. The SiN_x mask is subsequently removed using Buffered Hydrofluoric Acid (BHF).

The gratings in the SG-DBR sections are defined in the passive 1.4Q layer using a Methane/Hydrogen/Argon (MHA)-based RIE, as shown in Figure 13(c). The targeted grating depth is around 100 nm and duty cycle is 50%. The gratings are patterned onto a high-resolution photoresist using Electron-Beam Lithography. The grating pattern is transferred to a 50 nm thick SiO_2 layer using CHF_3-based RIE, which, in turn, is used as a hard-mask for the MHA RIE step that etches the grating into the 1.4Q layer. The grating period is targeted to be ~240 nm so that the center wavelength of the SG-DBR laser is close to 1550 nm. The sampled gratings are used in both the front-side and back-side mirrors of the SG-DBR lasers. The front-side mirror consists of 5 grating bursts, each burst being 6 µm long, that repeat periodically with an interval of 61.5 µm. The back-side mirror consists of 12 grating bursts, each burst being 4 µm long, that repeat periodically with an interval of 68.5 µm. More details about the wide wavelength tuning using the Vernier effect achievable with SG-DBR lasers can be found in [16]. The SiO_2 layer is subsequently removed using BHF, and the sample is thoroughly cleaned in UV-ozone prior to the regrowth step.

This is followed by a regrowth step, as shown in Figure 13Figure 18(d). The regrowth layers comprise of a 50 nm thick UID InP spacer that helps prevent diffusion of Zn from p-doped cladding into the underlying MQW layers in the active regions and the 1.4Q layer in the passive regions of the OPLL-PIC, a 2000 nm of Zn-doped InP cladding, where the doping is 7e17 cm^{-3} in the lower half of the cladding and 1e18 cm^{-3} in the upper half of the cladding, a 100 nm thick Zn-doped (1e19 cm^{-3}) InGaAs contact layer followed by a 200 nm thick Zn-doped (1e18 cm^{-3}) sacrificial InP cap layer, on the top of the wafer, which is used to protect the thin InGaAs contact layer during the processing steps prior to metallization. The p-doping in the InP cladding layer is decreased closer to the waveguide core in order to reduce the free-carrier-induced optical loss.

Following the regrowth, surface-ridge waveguides are etched, as shown in Figure 13 (e). First, an MHA-based RIE using a 100 nm thick SiN_x hard mask is used to etch the waveguides to a depth of ~ 1.5 µm below the regrown InGaAs layer. Following the dry etch, the surface ridge waveguide is further etched by a $HCl:H_3PO_4$ wet etch cleanup so that the rest of the p-doped InP cladding is removed. The 1.2Q layers directly above the MQW layer in the active regions and directly above the 1.4Q layer in the passive regions act as etch-stops for the selective wet-etch. All waveguides deviate less than 7° from the normal to the major plane, so that minimal undercutting of waveguide walls is observed. The waveguide widths are varied across different OPLL-PICs between 2 µm and 3 µm. Waveguide sections for input and output coupling of light are curved by 7° and their widths are tapered to 5.5 µm in order to minimize facet reflections. In addition, anti-reflection coatings are applied to the facets after the processing steps are completed.

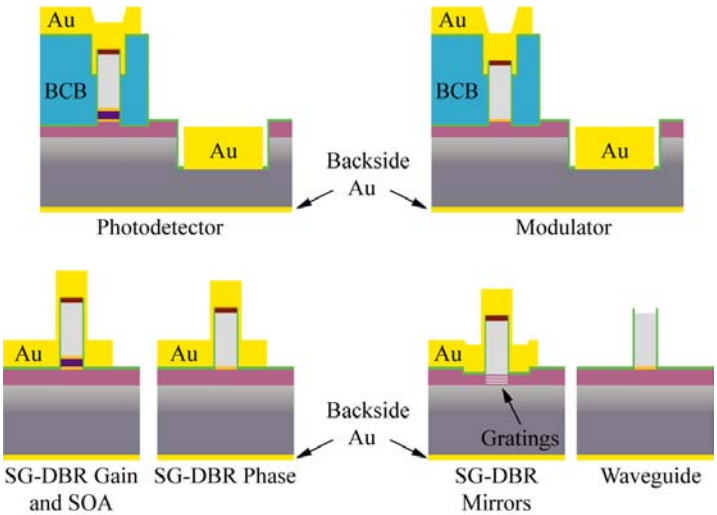


Figure 14. Schematics showing cross sections of various components of the fully processed OPLL-PIC.

The processing steps that follow the ridge waveguide etching are fairly common and not necessarily characteristic of our integration platform. Here, we summarize the remaining steps. Figure 14 shows various sections of our PIC after these processing steps have been completed.

First, a thick photoresist is patterned so that it covers the entire sample except ~12 μm on each side of the ridge waveguides sections that form the high-speed modulators and high-speed photodetectors. The waveguides are still protected by SiN_x hard mask that was used to etch the surface ridges in the previous step. MHA-based RIE is used to remove the top 20 nm thick 1.2Q SCH layer and approximately 80 nm of the underlying 1.4Q layer. Both of these layers contain Zn atoms that diffuse from the p-doped InP cladding during regrowth. These Zn atoms can considerably increase the capacitance for the detectors and modulators, necessating the dry etching of the top 100 nm of the quaternary semiconductor.

An additional 100 nm thick SiN_x layer is deposited and patterned to provide a hard mask for MHA-based RIE that is used to etch windows for top N-contact metallization. The etch is performed until it penetrates ~0.5 μm below the Si-graded-doped InP buffer into the heavily doped substrate. A thick photoresist covers the wafer everywhere except the N-contact metallization window regions. An electron-beam evaporator is used to deposit a Ni/AuGe/Ni/Au contact, which is patterned using the lift-off technique. The thickness of gold deposited during this step is only ~0.5 μm as more gold is added during the P-contact metallization step. As illustrated in Figure 14, the top N-contact is made only for fast devices, *i.e.*, photodetectors and modulators, which can be accessed by direct RF probing. N-contact for the remaining devices is achieved by back-side metallization at the end of processing. The N-contacts are annealed at 430 ºC for 30 s. After the top N-contact metallization, a thin SiN_x layer is deposit and photo-sensitive BCB is spun, developed, and cured at 250 ºC. This leaves BCB in places that will be underneath the P-contact metal pads and traces running along the lengths of the high-speed photodetectors and modulators and covering the surface ridges in these regions. Along with the capacitance reduction etch, the BCB further reduces the capacitance of these devices to the extent that should enable their operation at frequencies far exceeding 10 GHz. An additional thin SiN_x layer is deposit after BCB patterning. Thus, the BCB is sandwiched between thin layers of SiN_x, shown as thin green lines in Figure 14, for better adhesion to the semiconductor surface below as well as the P-contact metal on top.

Three different types of P-contact metal vias need to be opened in the top SiN_x layer prior to the P-contact metallization. First, vias are formed by removing the SiN_x layer above N-contact metal. This is accomplished by patterning photoresist to cover the sample everywhere except over the N-contact metal and dry etching the SiN_x layer above the N-contact metal using CF_4/O_2-based RIE. The next via is formed by removing the SiN_x layer on top of all the ridge waveguide sections except those covered with BCB. To open this via, photoresist is partly developed around the waveguides and partially etched back using O_2-based RIE until the ridge tops are exposed. CF_4/O_2-based RIE is then used to etch the SiN_x layer and expose the InP cap layer that is on top of the ridge waveguides. The remaining SiN_x on the sidewalls of the ridge and over the rest of the wafer is protected by photoresist during this step. Finally, vias through the BCB layers are opened using a two-step process. A via that is somewhat wider than the waveguide is etched using CF_4/O_2-based RIE to expose the ridge top underneath BCB and the SiN_x layers. SiN_x is then re-deposited to fill in any openings that typically develop between the waveguide sidewalls and BCB, and a new via that is narrower than the waveguide is dry etched until the BCB and SiN_x layers are completely removed thereby exposing the InP on the top of the ridge.

At this point the sacrificial InP cap layer is removed using HCl:H_3PO_4-based wet etch everywhere along the ridge waveguides, thus exposing the InGaAs contact layer. Standard Ti/Pt/Au P-contact metal is deposited by electron-beam evaporation, where gold thickness is over 2 µm. During the deposition, the sample is mounted to a rotation stage tilted at ~30º for maximum sidewall coverage. The P-contact metal is patterned using the lift-off technique. The thermal annealing is done at 400 ºC for 30s.

After the P-contact metallization, the SiN_x layers and the sacrificial InP cap layer are removed from the top surfaces of all waveguide ridge sections that are not covered by P-contact metal. Consequently, the top InGaAs contact layer is removed from the ridge tops in these sections using a H_3PO_4:H_2O_2:H_2O-based selective wet etch. SiN_x layers protect the top 1.4Q layer on each side of the ridge during this etch step. A thick photoresist is then patterned so that it covers the entire wafer except ~ 12 µm on each side of the ridge waveguide. The sample is then subjected to proton implantation which occurs over the regions that are not covered by P-contact metal or photoresist. Proton implantation along with the removal of the InGaAs contact layer increase the electrical isolation between neighboring devices and reduces the free-carrier-induced optical loss.

The sample is then thinned to a thickness of ~ 130 µm, for the ease of cleaving. Back-side Ti/Pt/Au metallization is performed using electron-beam evaporation, where the thickness of gold is around 0.3 µm. The thermal annealing is done at 380 ºC for 30s. The sample is cleaved into bars along facets that have the waveguides for input or output coupling to an optical fiber. Anti-reflection coatings are applied to these facets to further reduce reflections. Individual devices are then cleaved and mounted on carriers and wire-bonded.

5.2.Fabrication

Three quarters were processed. Figure 15 is used to explain these steps and the integration platform in general.

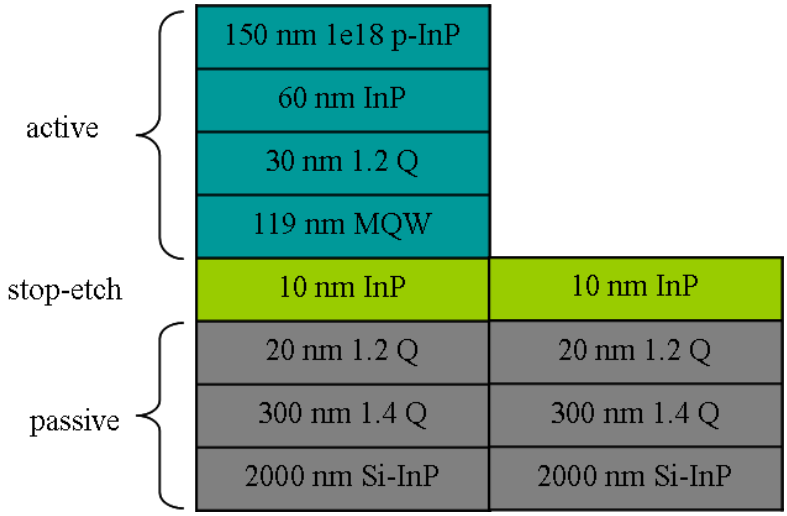


Figure 15. The base structure before (left-hand side) and after (right-hand side) wet etch of the active layers.

Figure 15 shows the base structure of the fabricated PIC before (left-hand side) and after (right-hand side) the top active layers have been removed by wet etching, where the 10-nm-thin InP layer is used as a etch stop layer. Following removal of the top active layers (often referred to as offset quantum wells), grating will be dry-etched in the areas of the sample containing back and front SGDBR laser mirrors. Following the dry etch of the gratins, the samples are submitted to p-InP cladding regrowth, as shown in Figure 16.

On two of the three samples being processed, the grating bursts have been directly written by e-beam (first written on a SiO_2 hard mask), while on the remaining sample, the grating bursts are achieved by holographic exposure, after windows have been opened in SiN_x in places where grating dry etching will take place. In both cases the gratings are about etched about 80 nm deep into the semiconductor, and they have a pitch of about 234 nm. Figure 17 shows the active regions, and the grating bursts that have been done by holography and dry-etched in the semiconductor. In this picture, SiN_x has not been removed yet. Similarly, Figure 18 shows the e-beam-written grating bursts after resist development. In this case, the gratings bursts are made narrower to save time during e-beam writing.

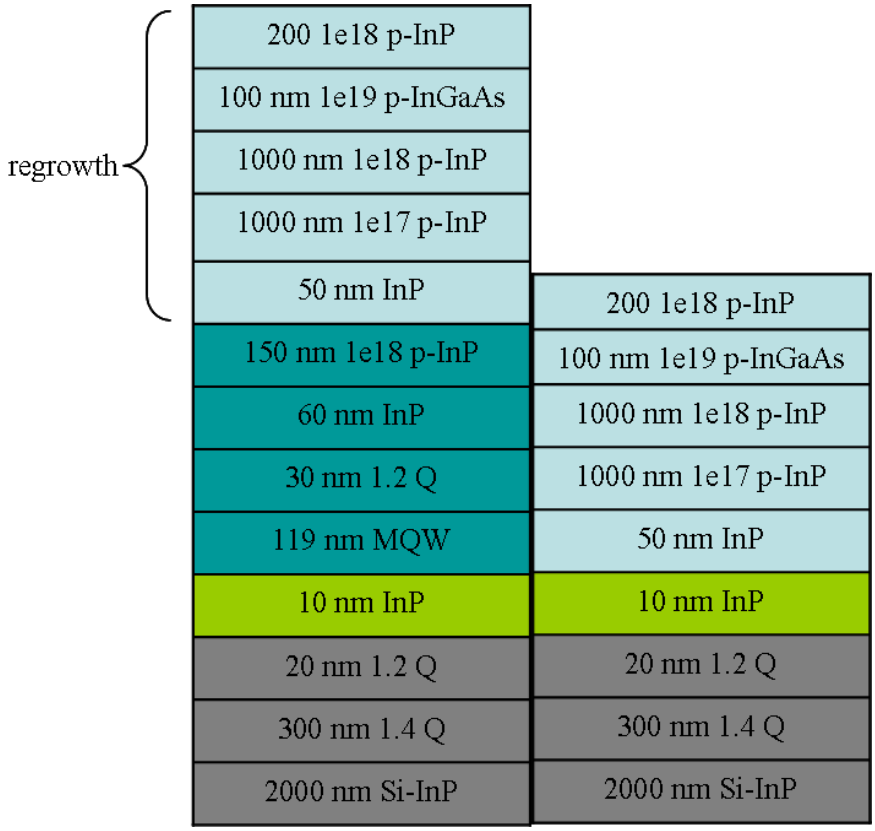


Figure 16. Active (left-hand side) and passive (right-hand side) regions after regrowth.

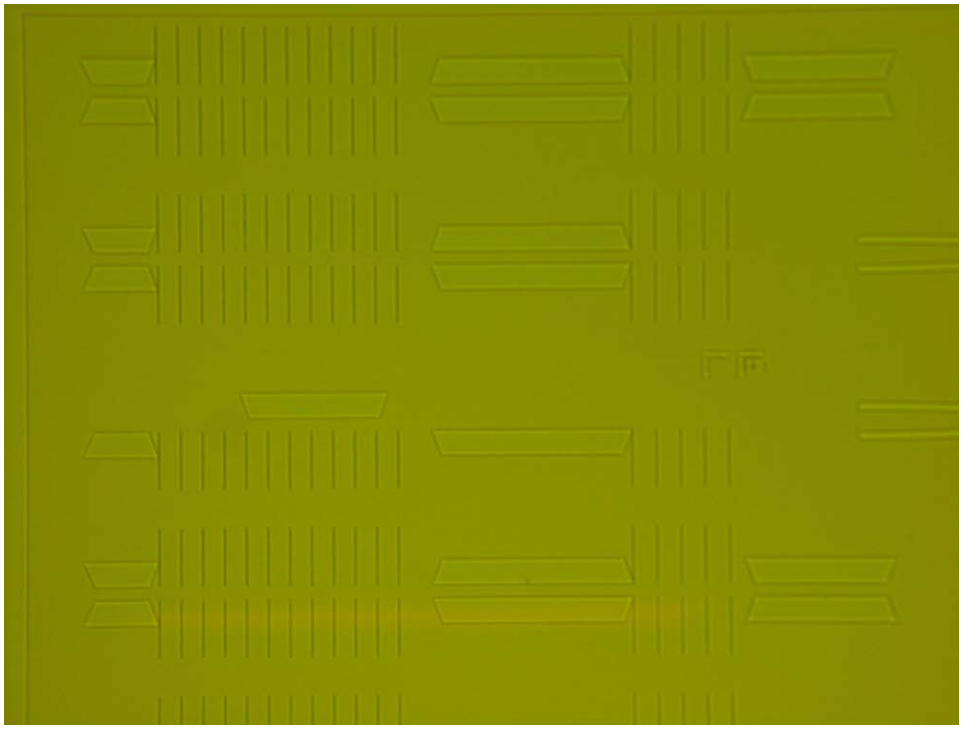


Figure 17. Holography grating bursts etched in the semiconductor, before removal of SiN_x.

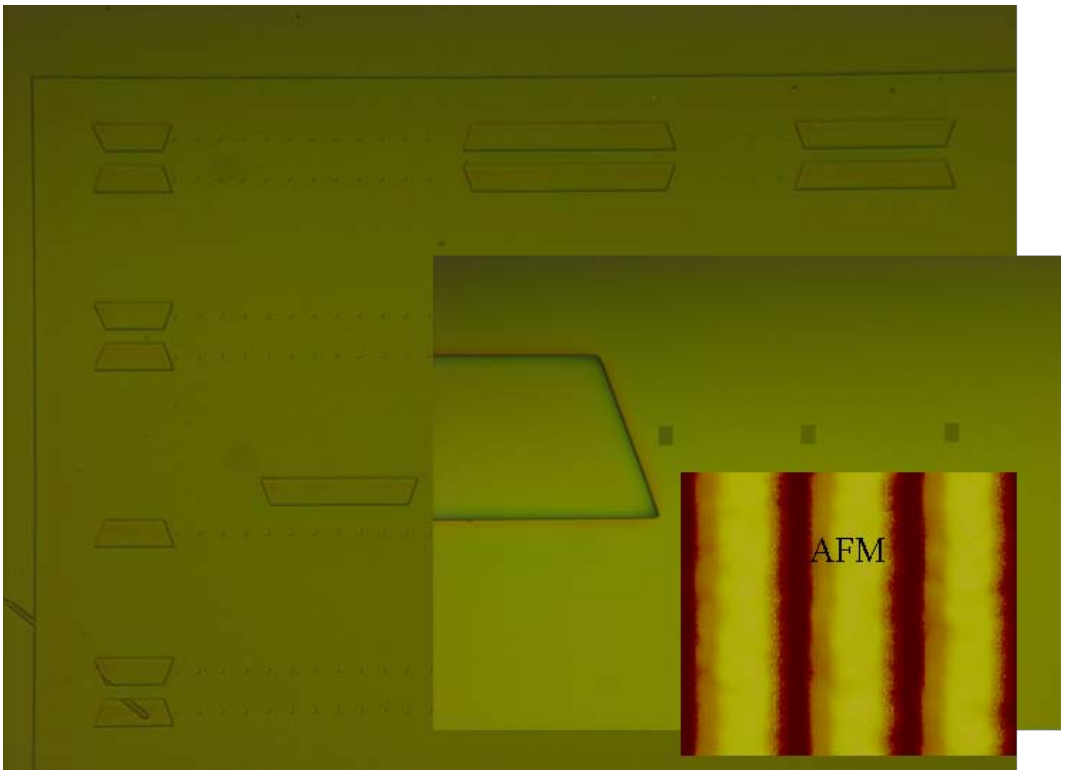


Figure 18. E-beam grating bursts developed in e-beam resist.

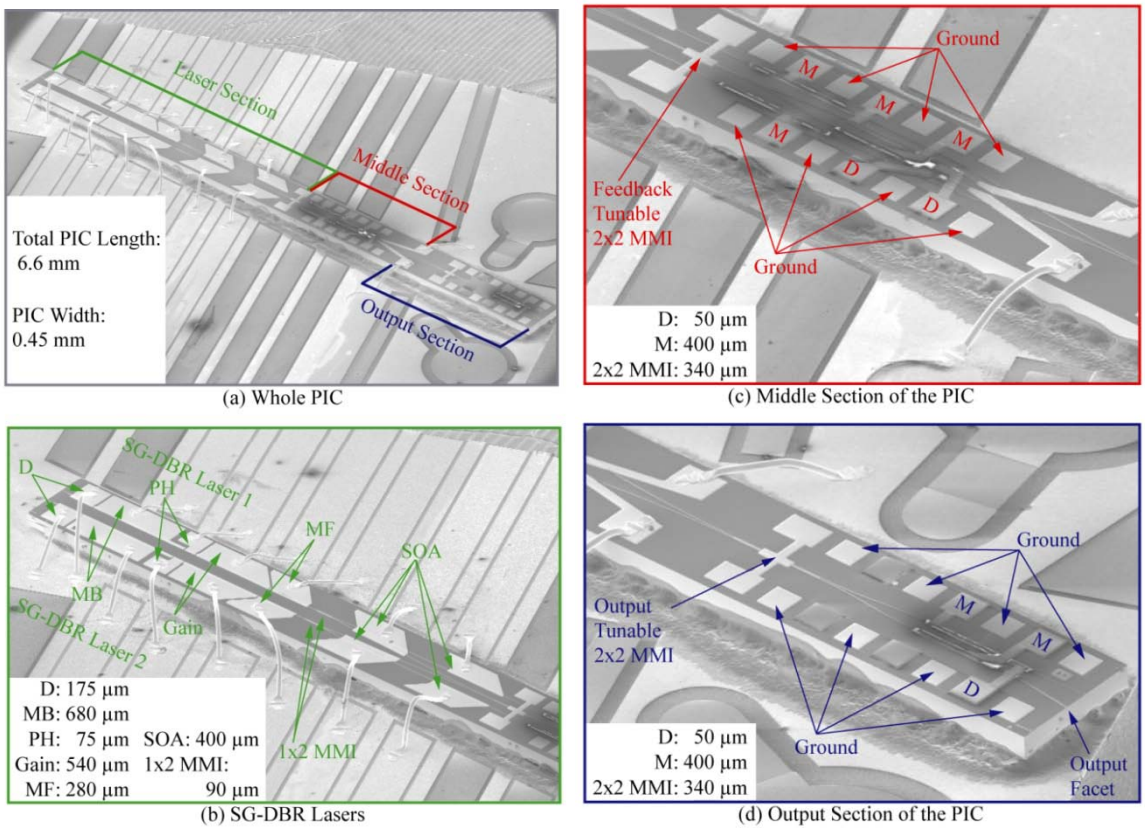


Figure 19. SEM images of the OPLL-PIC and its various sections.

Figure 19(a) shows a Scanning Electron Microscope (SEM) image of the fabricated OPLL-PIC based on the schematic shown in Figure 11(b), which enables offset locking, after it has been mounted on a carrier and wire-bonded. The distinct OPLL-PIC sections mentioned above are marked for identification. The OPLL-PIC is 6.6 mm long and 0.45 mm wide.

The Laser Section of the OPLL-PIC is shown in greater detail in Figure 19(b). The abbreviations used in labeling the various components of this section are explained in Figure 9. This section also includes the two 1×2 MMI splitters and the four SOAs. Some variations of the PIC were designed to have only two SOAs, one for each laser, placed at inputs of the 1×2 MMI splitters.

Figure 19(c) shows the Middle Section of the OPLL-PIC. The 2×2 MMI in this section can be tuned by current injection. The modulator and photodetector at the output of the 2x2 MMI connect to RF pads that are arranged in a G-S-G-S-G-S-G configuration for direct probing, with 150 µm pitch and 100 µm × 100 µm surface area per pad. Two 200 µm long curved (7) active sections with grounded pads, absorb light that is not absorbed in the two photodetectors. Figure 19(d) shows the Output Section of the OPLL-PIC. The two modulators and the photodetector at the outputs of the 2x2 MMI connect to RF pads that are arranged in the same way as those in the Middle Section of the OPLL-PIC, except that here there are three unused pads. The output waveguides that enable coupling into an optical fiber are angled at °7with respect to the direction normal to the cleaved facet, and anti-reflection coatings are applied in order to minimize facet reflections.

6. TASK 3, ELECTRONIC IC DESIGN

Task Description: *In accordance with task 1, feedback electronics will need to be designed with the required filter response for stable laser phase-locking. Generate designs using standard silicon foundry processes and fabrication.*

6.1. Overview of design options:

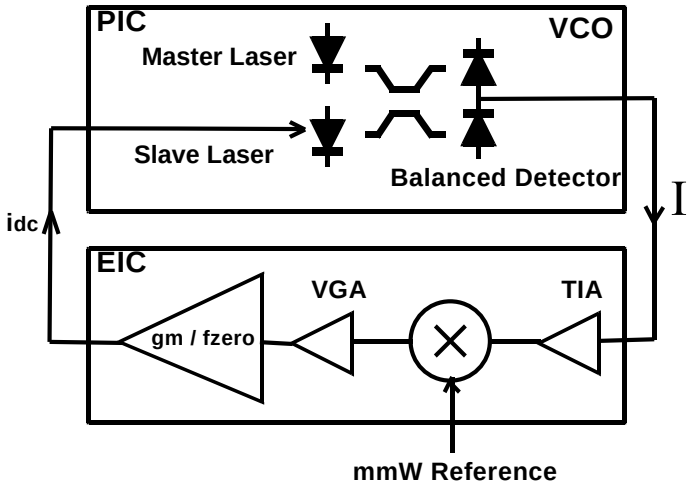


Figure 20. Schematic of the standard loop electronics design.

In the optical phase locked loop the Photonic IC serves as a VCO with the output being a current proportional to the phase difference between the master and slave lasers.

$$I \alpha \cos(\varphi_m - \varphi_s) \tag{10}$$

where φm and φs represent the phase of master and slave respectively. This current is converted to voltage signal using a TIA. The TIA bandwidth should be much more than the desired loop bandwidth required for locking the two lasers. The frequency of this voltage signal is the heterodyne frequency of the two lasers. The mixer shown in the above figure acts as a phase detector comparing the signal with mmW reference offset frequency and generating an error signal. The VGA is included in the loop to be able to control the loop gain of the PLL. There is also a loop filter which integrates the phase error to a dc current required to drive the laser and change its frequency. A zero is introduced in the loop filter to compensate for the roll off in the VCO frequency response and provide additional phase and gain margin. In this setup the frequency of the slave laser is given as $\omega_S = \omega_M + \omega_{RF}$ OR $\omega_S = \omega_M - \omega_{RF}$

The goal is to be able to achieve a loop delay of around 100ps which corresponds to a loop bandwidth of 1GHz. In addition to the standard loop electronics design, a costas-loop feedback electronics design have also been outlined. The schematic for this design is outlined in Figure 21 below.

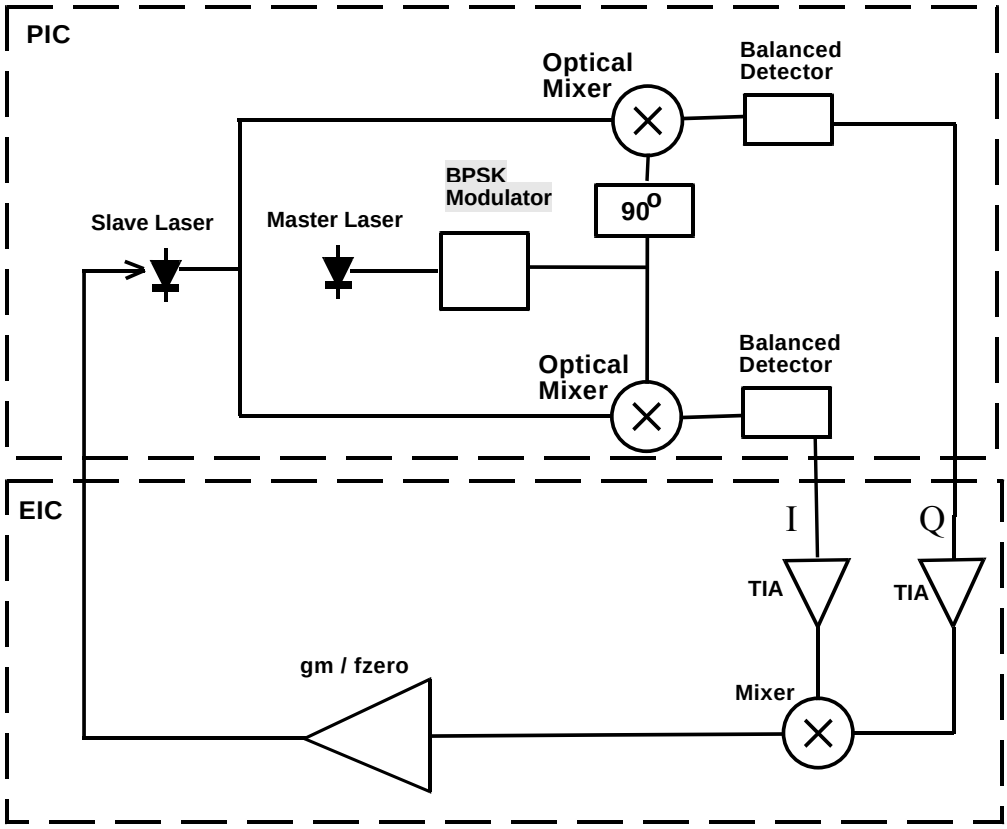


Figure 21. Schematic of the costa's loop electronics design.

For optimum flexibility in loop electronics design, a modular approach have been taken, where the different stages are externally connected using wirebonds. Figure 22 sows a picture of the fabricated SiGe chips. The modular approach lowers the risk and improves failure diagnosis with a small performance penalty in higher loop delay from chip interconnects. In the following, details of the design for each stage are given:

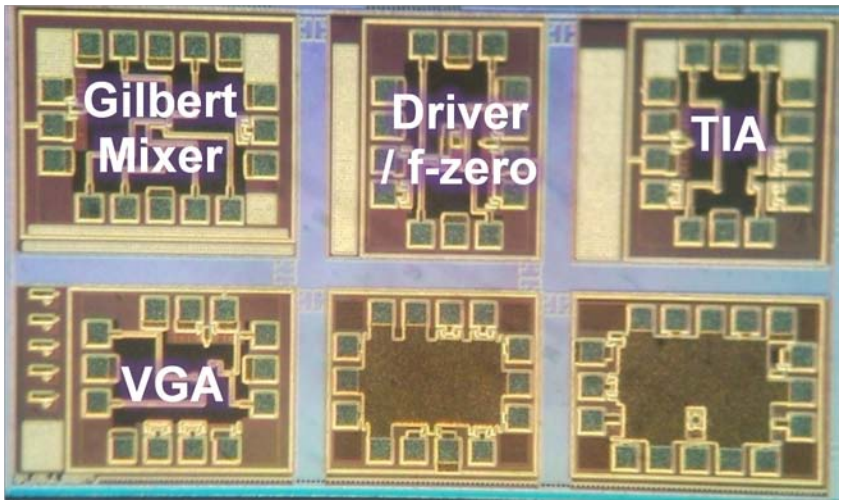


Figure 22. Picture of fabricated SiGe electronics.

6.2. TIA (Trans-Impedance Amplifier):

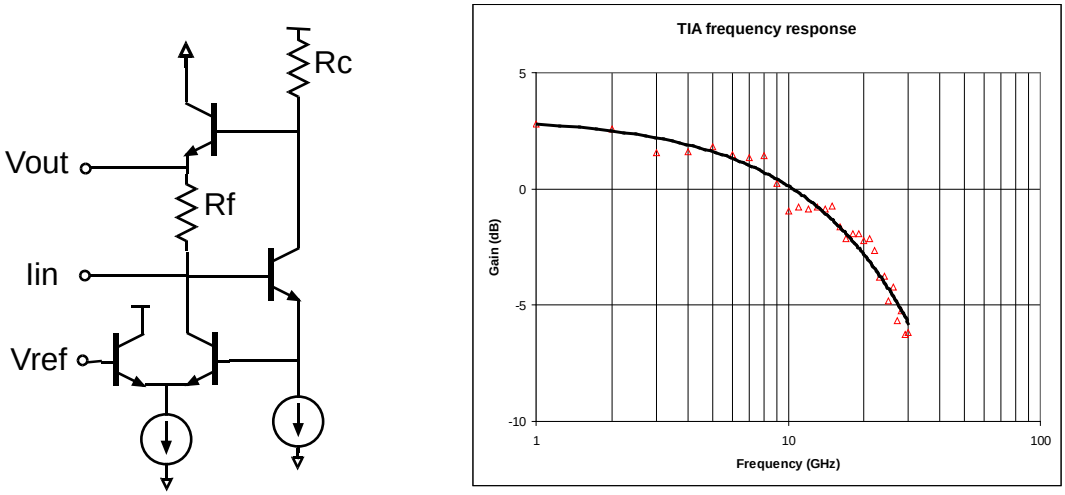


Figure 23. Left: TIA half Circuit. Right: Measured frequency response.

The TIA shown above has been implemented in IBM 7HP SiGe technology. The transimpedance Zt is given as

$$Zt = Rf\,(gm - 1/Rf) / (gm + 1/Rc) \cong Rf \qquad (11)$$

The measured Zt was found to be around 55Ω with a bandwidth of ~10GHz as can be seen from the frequency response. Common mode feedback circuit has been incorporated in the TIA design to take care of the changes in the DC bias currents from the photodetectors. The output DC conditions and the Zt remain unaltered with the variations in the input DC current. Figure 24 below shows the gain compression plots for the TIA

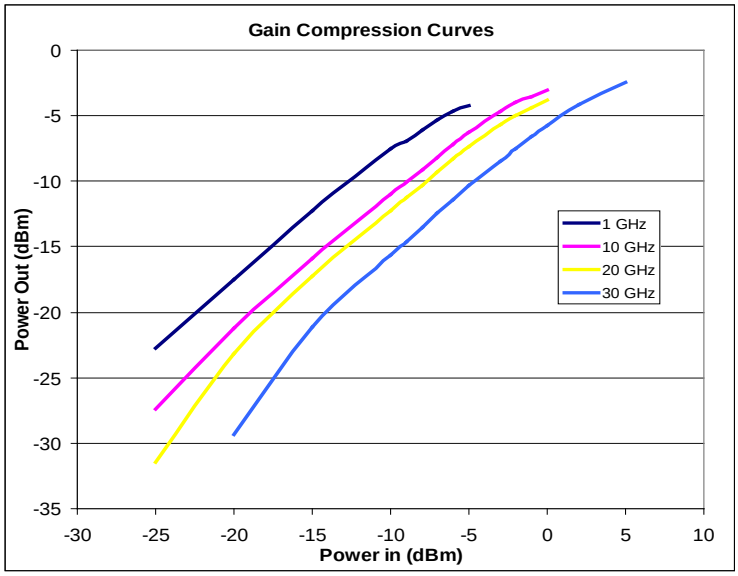


Figure 24. Measured gain compression plots for the TIA.

6.3. Variable gain Amplifier

The VGA has been introduced in the loop to be able to control the loop gain on the PLL. Also, the current from the balanced detector can vary a lot giving rise to changes in the amplitude at the output of the TIA. The large signal can cause gain compression of the following stages. To avoid gain compression the VGA can be used to reduce the loop gain. The VGA has also been implemented in IBM 7HP SiGe technology. The bandwidth of the VGA was measured to be ~10GHz with a gain of ~6dB, as seen below in Figure 25.

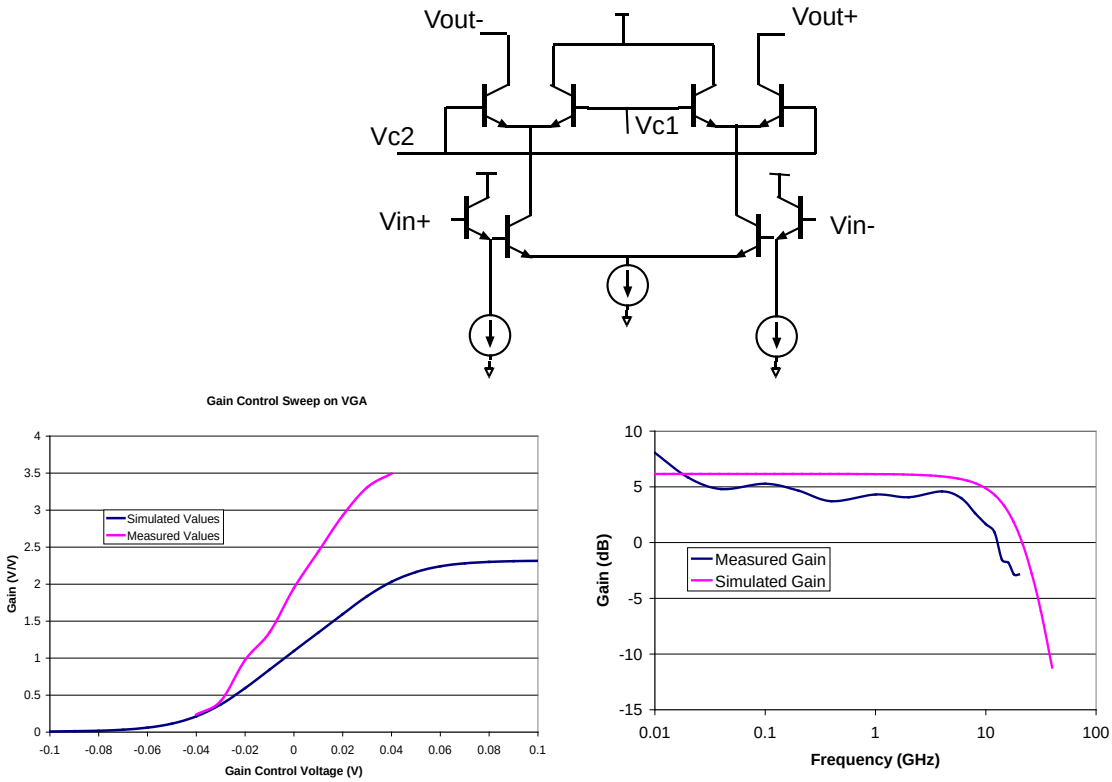


Figure 25. Top: VGA Circuit. Bottom: Measured gain and bandwidth of fabricated VGA.

6.4. The Gilbert cell Mixer

The gilbert cell mixer has been implemented in IBM 7HP SiGe technology and the circuit diagram is shown below. This can be used either as a phase detector or as a multiplier.

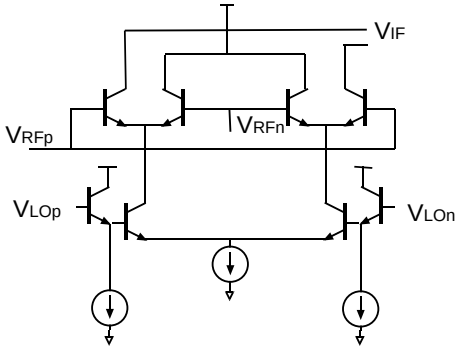


Figure 26. Schematic of Gilber cell mixer.

6.5. Laser driver/f-zero stage:

The last component fabricated is the laser driver / f-zero component. This is used to translate the output voltage of the VGA or mixer into a drive current for the laser tuning section. Additionally, it provides a zero frequency for stabilization of the loop, as discussed above in the summary for task 1. Figure 26 shows the measured compression point for the driver, well sufficient to drive the SGDBR laser phase section

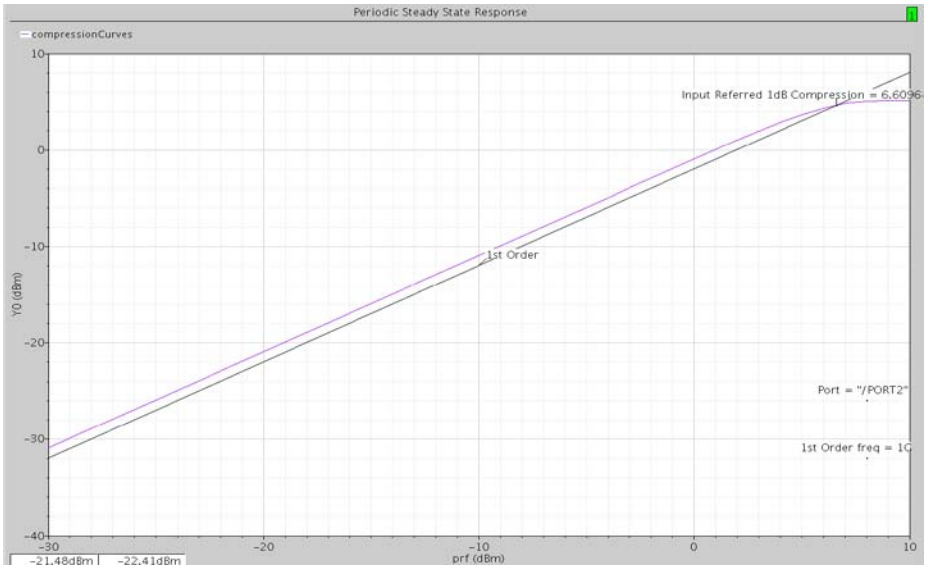


Figure 26. Measured 1dB compression point (1GHz) at 6.6096dBm for the f-zero/laser driver.

7. OPLL ASSEMBLY AND CHARACTERIZATION:

Task description: *Identify and obtain commercial low latency feedback electronics. Once electronic and photonic IC's chips are available begin characterization by verifying operation of individual optical subcomponents and the response of feedback electronics. Mount chips on common ceramic test carrier. Wire bond DC connections, including appropriate bypass capacitors and inductors. Ribbon bond RF connections. Verify frequency tuning capability of slave. Verify feedback filter function. Advance to optical phase-locking experiments. Measure phase-noise performance of the locked laser. Compare results to simple model. First systems demonstrations include offset-locking laser heterodyne source with RF modulation in the 10-40GHz range with >90% modulation depth. To show the feasibility for multilevel mmW data modulation, sufficient signal to noise ratio must be supported. This can be quantified as a phase error variance of less than 0.01 rad^2 and a mmW carrier to noise ratio higher than 135dB/Hz (over the data bandwidth). Finally; simple 10Gbps data modulation (PSK or ASK) will be encoded to the generated mmW to show feasibility for the proposed optical mmW source concept.*

7.1. 11-month OPLL performance metrics:

By the end of this seedling, the following performance metrics will have to be demonstrated to show feasibility for the optical mmW source. These have been derived from the requirement of being able to carry 100Gbps multilevel modulation.

Table 3: Target performance metrics

Generated Heterodyne Frequency:	10GHz – 40 GHz
mmW modulation depth:	>90%
Phase Error Variance:	<0.01 rad^2
CNR	135 dB/Hz
mmW-carrier data rate:	10 Gbps

7.2. Base component testing:

Besides the fact that it is a well established technology, there are at least four important characteristics of the SG-DBR laser that make it a very attractive choice for its use in an OPLL.

First, SG-DBR lasers have in excess of 40 nm of quasi-continuous wavelength tuning range, as shown in the optical spectrum analyzer spectra plotted in Figure 28. In this figure, one of two on-chip SG-DBR lasers is tuned to a constant wavelength, while the wavelength of the other on-chip SG-DBR laser is detuned away from that wavelength in increments of ~ 5 nm. This wide wavelength tuning range enables the OPLL-PIC to generate a heterodyne beat frequency that spans from DC to over 5 THz.

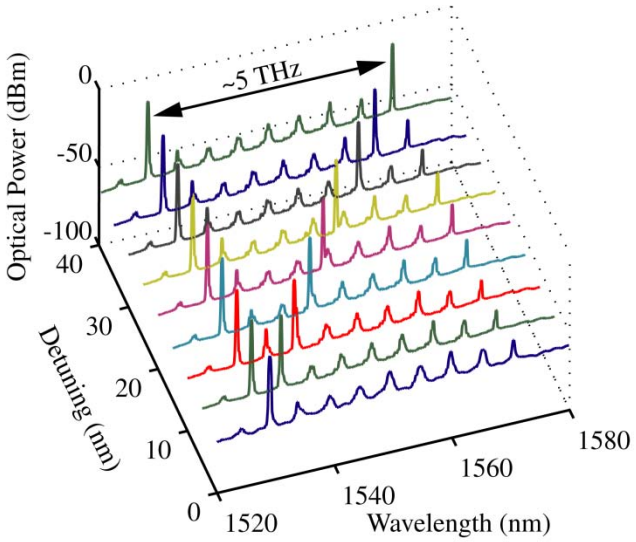


Figure 27. Optical spectra obtained by heterodyning two integrated, unlocked widely tunable SG-DBR lasers.

Second, the FM tuning mechanism of the SG-DBR laser is very efficient. Unlike Distributed Feedback (DFB) lasers, which are tuned by current injection into the laser gain section, in SG-DBR lasers, the tuning is achieved by current injection into a small, separate, passive phase section. The DC FM sensitivity can be as high as 20 GHz/mA for this tuning mechanism, which is over an order of magnitude greater than the 1-3 GHz/mA DC FM sensitivity reported for a DFB laser optimized for use in OPLL applications [3]. The large FM sensitivity directly translates into a large feedback loop gain and thus helps improve OPLL stability.

Third, and perhaps the most important advantage of the SG-DBR laser is that, unlike in a typical DFB laser, there is no sign change in the FM phase response. The FM response has a 3 dB bandwidth of ~70 MHz, and no phase inversion is observed below this frequency. The phase inversion in a DFB laser occurs within its bandwidth at a frequency where the thermal effect becomes too slow to dominate frequency tuning with the corresponding red shift in the FM response so that frequency tuning becomes dominated by the carrier-injection effect and the corresponding blue shift in the FM response. It is very challenging to implement an OPLL feedback electronic circuit that can compensate for this phase inversion. The absence of phase inversion in the FM phase response of an SG-DBR laser is due to the fact that a) the small and efficient phase tuning pads require small currents for tuning, thereby reducing the thermal effects, and b) the phase section is composed of the passive material that has a band gap larger than that of the active material so that the accumulation of carriers is very efficient as they cannot be depleted by stimulated emission.

Fourth, the linewidth of an SG-DBR laser is dominated by low-frequency jitter [17], which is not very difficult to compensate with the large bandwidth of an integrated OPLL, which as we will show below is at least 300 MHz.

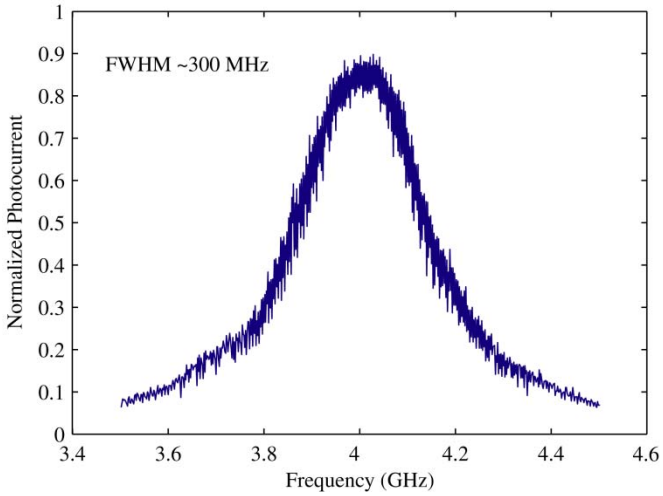


Figure 28. Composite linewidth measured from the heterodyne beat of the two integrated, unlocked SG-DBR lasers.

We note that the Shawlow-Townes linewidth limit for a typical SG-DBR laser is typically below 1 MHz [17]. However, the linewidth that we measure with a 30-μs-delay self-homodyne technique is in the range 10 MHz to 50 MHz, varying with mirror setting, which is dominated by low-frequency jitter noise. This linewidth would be hard to compensate with an OPLL that is not integrated. Figure 28 shows the combined linewidth from the heterodyne beat of two unlocked, integrated SG-DBR lasers by combining their outputs at an offset frequency. The combined linewidth of ~300 MHz is measured using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. This wide linewidth is associated with low frequency current noise on the tuning port, and this is normally removed with a large capacitive load in cases where rapid tuning is not required.

7.3. Proof-of-Concept Experiment:

We perform two experiments in order to demonstrate proof-of-concept operation of the OPLL: homodyne locking and offset locking of the two monolithically integrated SG-DBR-lasers, as presented in subsections 7.4 and 7.5 below. Before presenting the details of these two experiments, we first present the basics of the electronics used in the feedback loop.

Figure 30 shows the schematic of OPLL-PIC including the feedback electronic circuit when used in the homodyne locking experiment, and Figure 30 shows the corresponding optical image. The electronic circuit is built around a Field Effect Transistor (FET). One of the two photodetectors in the Middle Section of the OPLL-PIC is used to detect a phase error signal between the two lasers, which is converted to an amplitude error signal in the 2×2 MMI. The reverse-biased current signal generated by this photodetector is amplified by the FET and converted into a forward-biased current signal needed to control the injection of carriers into the phase section of the slave SG-DBR laser.

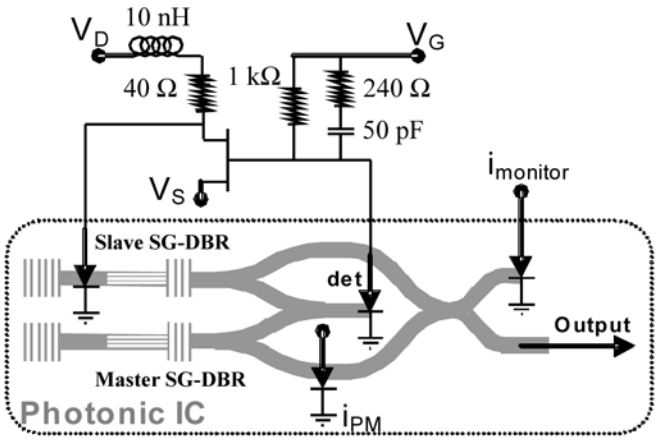


Figure 30. Schematic of the homodyne locking experimental setup.

We design the detector load to provide a second order loop transfer function with lag compensation. The FM response of the SG-DBR laser has a 3-dB point around 70 MHz. The LR circuit that loads the laser phase section is designed to have a zero close to the laser's pole, compensating its FM response and making it a more controllable device. The RC circuit that loads the photodetector is designed to provide the following function. The larger of the two resistors dominates at frequencies closer to DC and ensures a large locking range. The other resistor dominates at frequencies closer to the 3-dB point and provides the desired zero needed to improve the stability of the loop for the higher frequencies where the gain becomes unity. The resulting loop bandwidth that we measure is ~300 MHz. Similar to a voltage-controlled oscillator an RF phase-locked loop, the laser itself acts as an integrator, which means that the rest of the electronics is required to provide a single pole to realize a second order loop.

7.4. Homodyne Locking

As mentioned above, the schematic and optical image corresponding to the homodyne locking experiment are shown in Figure 30 and Figure 31, respectively. No current is applied to the back-side or the front-side mirror of the two SG-DBR lasers, so that they lase at their untuned wavelengths, which are close to 1542 nm. The random phase variation between the two lasers translates into an intensity modulated error signal at the output of the 2x2 MMI in the Middle Section of the OPLL-PIC and finally into a current error signal at the output of one of the photodetectors that is connected to the feedback loop. The error signal then passes through the electronic circuit and tunes the frequency of the slave laser so that it is matched to that of the master laser, where the slave laser effectively plays a role of a current-controlled oscillator.

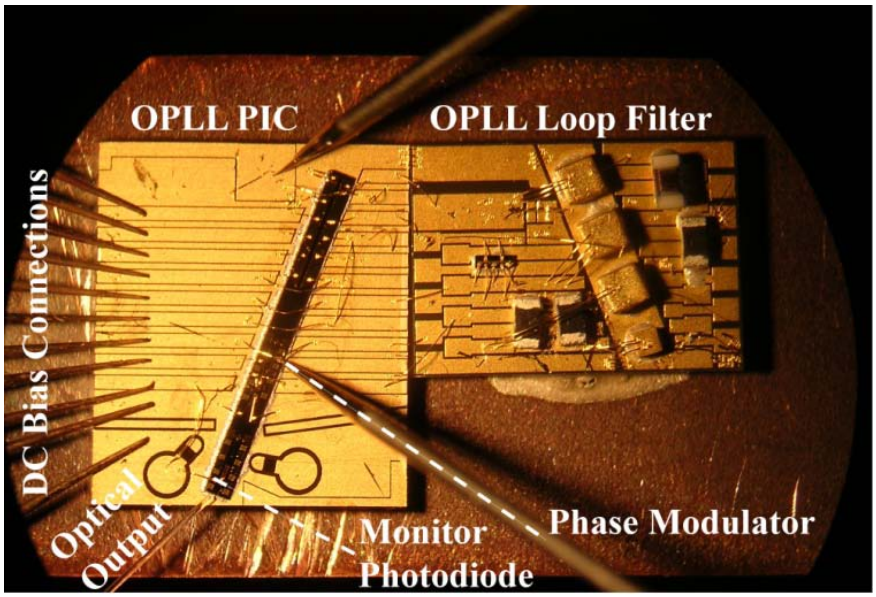


Figure 29. Optical image of the homodyne locking experimental setup.

In order to bring the OPLL from an unlocked state into a locked state, we inject appropriate bias currents into the phase section of the one of the SG-DBR laser until its frequency is within the feedback loop bandwidth, i.e. ~300 MHz, to that of the second SG-DBR laser. The bias current is adjusted until the noise spectrum measured at the optical output of the OPLL-PIC changes as shown in Figure 32, which indicates that the OPLL-PIC has fallen into a locked state. Figure 32 also reveals the expected presence of the 300 MHz resonance frequency peak, above which the OPLL provides a positive rather than negative feedback and becomes unstable. The data is acquired using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. The uncompensated low-frequency noise below the resonance frequency peak is mainly due to OPLL-PIC's AM noise that can be effectively cancelled using feedback from a balanced photodetector pair (implemented on the PIC, but not used here) rather than a single photodetector.

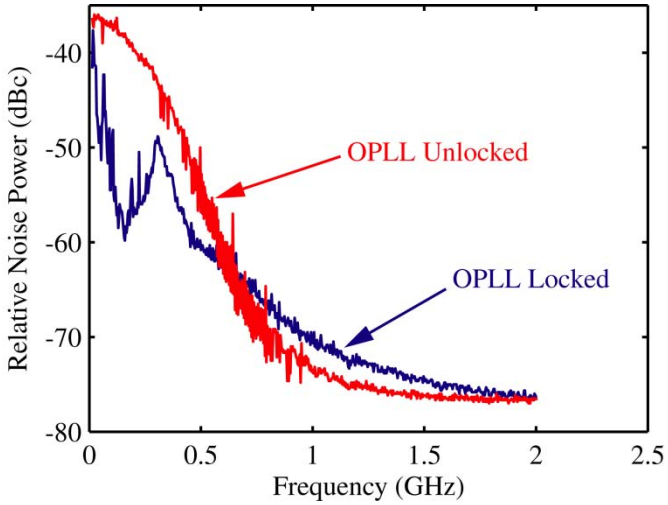


Figure 30. Noise spectra measured at the optical output of the OPLL-PIC in the homodyne locking experiment.

To further confirm the homodyne locking, we inject current into one of the modulators and continuously adjust the phase of the light from one of the SG-DBR lasers. This modulator is part of the waveguide that directs light toward the 2x2 MMI in the Output Section of the OPLL-PIC and is not the feedback-loop. This phase modulator allows us to independently modulate the phase of one SG-DBR laser output while leaving the phase of the second SG-DBR laser unchanged. When the OPLL is in the locked state, the two lasers are coherent with respect to each other. By changing the phase on one of the lasers, the interference between the two lasers in the 2x2 MMI in the Output Section of the OPLL-PIC shows the characteristic interference that is observed from a Mach-Zehnder Interferometer (MZI), which converts phase modulation to amplitude modulation. When the OPLL is not locked, the two lasers are not coherent with respect to each other and their interference in the 2x2 MMI does not exhibit the phase to amplitude modulation response that is characteristic of an MZI.

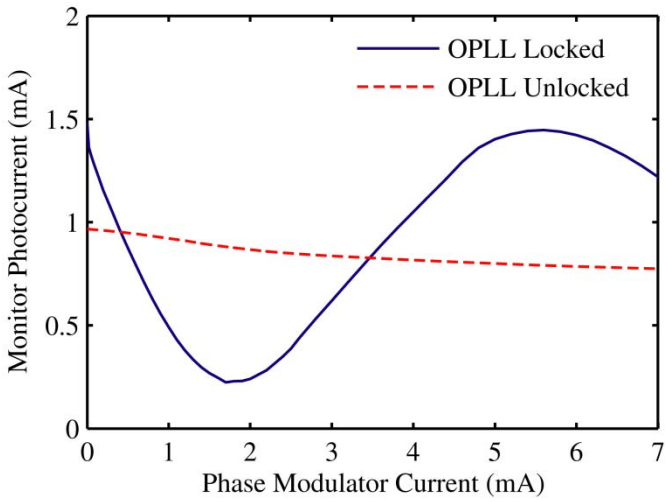


Figure 31. Phase-to-amplitude modulation conversion observed for the locked and unlocked states of the OPLL for homodyne locking of the two SG-DBR lasers.

Figure 33 illustrates this behavior for both locked and unlocked states of the OPLL. In both cases, we see a small intensity modulation characteristic for our modulators when operated in the forward bias. Also, the half-wave current (I_π) needed for switching the interference between "on" and "off" states is ~4 mA, which is consistent with other measurements performed on similar phase modulators. The limited extinction ratio (~8 dB) observed for the constructive versus destructive interference is due to unequal optical power reaching the 2x2 MMI.

7.5. Offset Locking

The same PIC and electronic circuit that were used in the homodyne experiment are also used in the offset locking experiment. To demonstrate offset-locking of the two monolithically integrated SG-DBR lasers, we apply a reverse bias phase modulation to one of the modulators that is connected to the output of the 2x2 MMI in the Middle Section of the OPLL-PIC and is a part of the feedback loop, as shown in Fig 1. As this phase modulator output is only connected to the integrated detector pair used for the feedback circuit, the OPLL-PIC output signal does not contain any modulation sidebands. In this case, we use the reverse bias amplitude modulation

based on the Franz-Keldysh effect because the GHz-range modulation frequency that we need far exceeds the bandwidth (~100 MHz) of the modulator in the forward-biased current-injection mode. In our offset-locking scheme, the carrier frequencies from both lasers are simultaneously modulated, which generates two modulation sidebands corresponding to either laser's carrier frequency. When the frequency separation between the two SG-DBR lasers equals the modulation frequency, the detected photocurrent will contain a phase-dependent DC component, and sideband locking of the two lasers becomes possible. Mixing of the two laser frequencies and their sidebands occurs in the photodetector, which generates a corresponding current error signal to the feedback electronics and the phase section of the slave laser whenever there is a random phase walk-off between a center frequency of one laser and a sideband of the other laser. The power in the sidebands is smaller in comparison to the power at the center frequencies of the laser. Consequently, the extinction ratio of the corresponding interference is smaller than for the homodyne OPLL, producing a weaker error signal. To compensate for this, to generate as strong modulation sidebands as possible, the power applied to the modulator used in offset locking is between 10 dBm and 15 dBm.

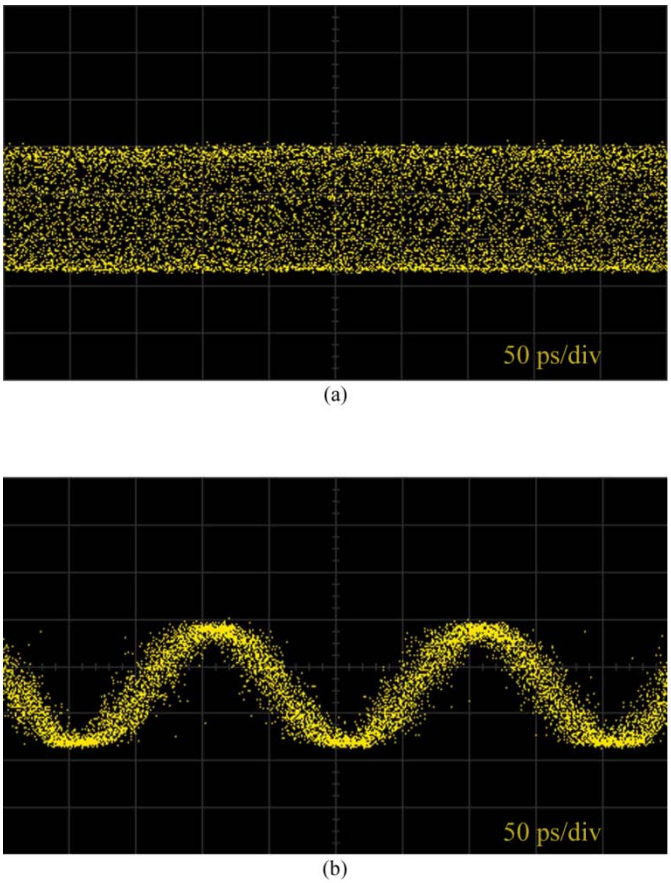


Figure 32. Oscilloscope traces observed at the optical output of the OPLL-PIC in the heterodyne locking experiment when the OPLL is (a) unlocked and (b) locked.

Figure 34(a) and (b) show an oscilloscope trace of the OPLL-PIC's optical output before and after 5 GHz offset locking of the two SG-DBR lasers, respectively. The oscilloscope is triggered by the 5 GHz modulating signal. Before locking, the phase of the beat varies randomly and only an envelope of the beat is observed in Figure 34 (a). After phase-locking, a coherent beat signal

is generated, as observed by the oscilloscope trace in Figure 34 (b). The very similar amplitudes of the unlocked and locked signals in these two figures (plotted on the same vertical scale) reveal that almost 100% of the laser power is in the locked state once the OPLL is locked.

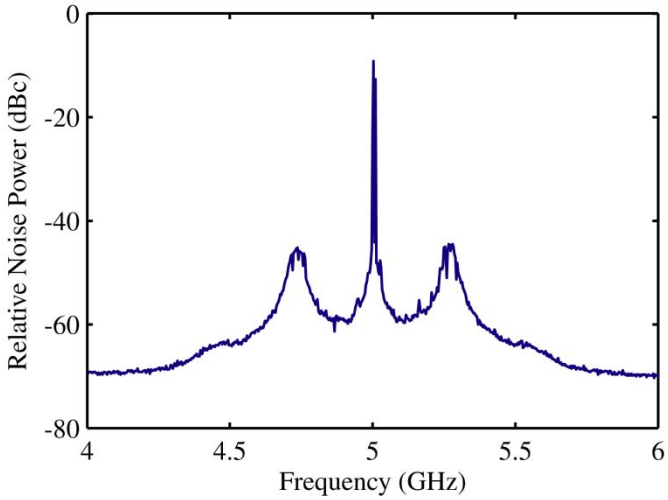


Figure 33. Noise spectrum measured at the optical output of the OPLL-PIC in the heterodyne locking experiment.

In addition to the time domain representation of the locked beat shown in Figure 34(b), in Figure 35, we plot the corresponding frequency spectrum obtained using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. As expected, the spectrum is centered at the 5 GHz modulation frequency, surrounded by two peaks that are offset by ~300 MHz, corresponding to the bandwidth of the feedback loop. We obtained similar results for different offset frequencies up to 15 GHz.

Once offset locking is achieved, data modulation can be applied to one of the generated optical components from the heterodyne OPLL. After photomixing, optical modulation is then downconverted from optical frequencies to RF (or mmW/THz). Figure 36 shows a schematic for the generation of 50 Mbps PSK modulated 10.2 GHz RF carrier. The OPLL is operated in a heterodyne arrangement, as outlined above, generating a 10.2 GHz beat signal. The optical output from one of the lasers is then modulated in phase using one of the integrated optical modulators. Efficient and pure optical phase modulation is generated by operating the phase modulator in forward biased condition, where optical absorption is small, but efficient waveguide index change is ensured by carrier injection into the waveguide layer.

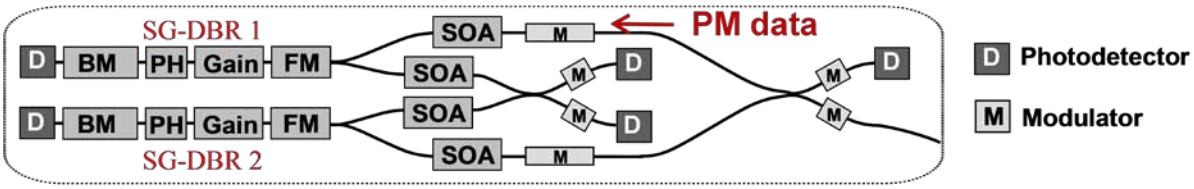


Figure 34. Experimental arrangement for generation of 50Mbit/s PSK modulated 10.2GHz carriers.

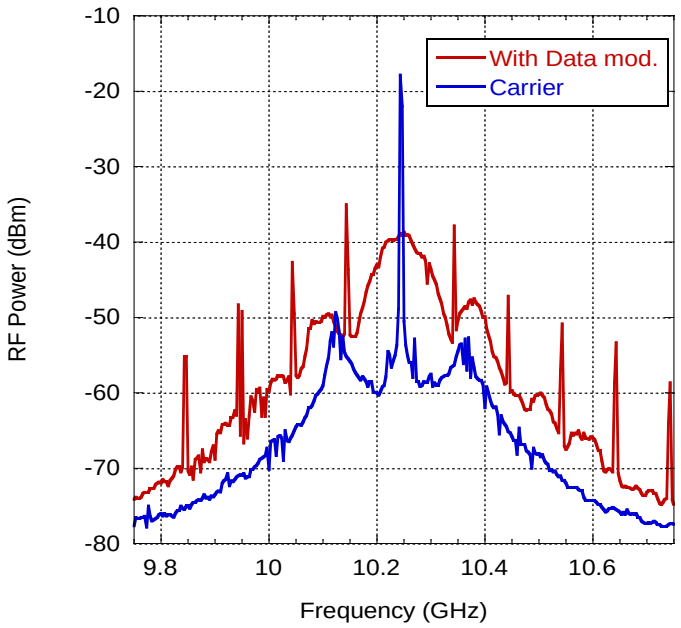


Figure 35. Detected RF spectrum with and without data modulation.

Figure 37 shows the detected RF spectrum for the optical heterodyne signal, with and without 50Mbps PSK modulation applied. The typical sinc-shaped spectral profile of a binary PSK modulated carrier is clearly observed. Figure 38 shows the demodulated eye diagrams. A synchronous demodulation scheme was used, i.e. the original RF reference signal used to lock the heterodyne OPLL was also used to demodulate the detected PSK modulated 10.2 GHz carrier after transmission and photomixing. A double balanced mixer was used to perform the RF demodulation, and a low-pass RF filter was used to filter away any carrier leakage. The eye diagrams are clearly visible, verifying the coherence performance of the heterodyne OPLL.

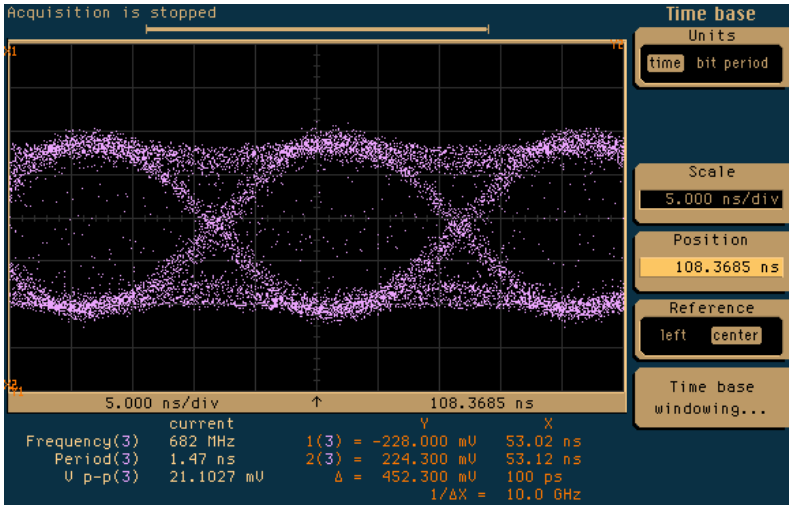


Figure 36. Synchronously demodulated PSK data.

8. CONCLUSION

In this seedling, we have successfully demonstrated the first monolithically integrated optical phase-locked loop photonic integrated circuit in which all of the optical components are integrated on the same InP platform, including: master and slave SG-DBR lasers, high-speed modulators, high-speed photodetectors, multimode interference couples/splitters, as well as interconnecting optical waveguides. Compared to the alternatives, monolithic integration an optical phase-locked loop is expected not only to provide a competitive performance, but also to make the technology more easily packaged and less expensive.

We have shown that, via monolithic integration, the phase-locked loop can be made sufficiently compact, and thus have a sufficiently wide bandwidth (300 MHz), to allow use of wide linewidth semiconductor lasers. We have further demonstrated suitability of SG-DBR lasers to be used as the master laser and the slave laser, *i.e.*, current-controlled oscillator, in this application. Most importantly, unlike the DFB laser, the slave SG-DBR laser does not suffer from a phase inversion in the FM frequency response, which is not easily compensated by the loop filter electronics. In addition, the slave SG-DBR laser offers a large phase tuning sensitivity, improving the gain and stability of the phase-locked loop. We have also shown that the detuning range of the master and slave SG-DBR lasers exceeds 5 THz, which enables the phase-locked loop to generate phase-stable optical beats at very high frequencies. This beat can be modulated with on-chip high-speed modulators and also converted into an electrical signal with on-chip high-speed photodetectors.

We have performed two experiments to demonstrate the proof-of-concept operation of the monolithically integrated phase-locked loop: homodyne locking and offset (5 GHz offset) locking of the master and slave SG-DBR lasers. We have shown that a simple electronic filter is sufficient to enable locking. The future versions of optical phased-locked loop will utilize both feedback photodetectors as a balanced pair in order to reduce laser amplitude noise. In addition, integrated feedback electronics will be implemented to further increase the bandwidth of the loop. Both of the changes are expected to significantly reduce the phase noise of the phase-locked loop. Finally, a heterodyne demonstration carrying data has been performed.

Table 4. Target and achieved OPLL performance metrics

	Target	**Achieved**
Generated Heterodyne Frequency:	10GHz – 40 GHz	2 GHz – 20 GHz*
mmW modulation depth:	>90%	>90%
Phase Error Variance:	<0.01 rad^2	0.03 rad^2 in 2GHz bw
CNR	135 dB/Hz	120 dB/Hz (at 1GHz offset)
mmW-carrier data rate:	10 Gbps	<200 Mbps

Table 4 shows the target and achieved OPLL performance metrics. Peak measured heterodyne frequency was limited by available measurement equipment, not inherent OPLL capabilities. Phase noise will be improved by implementing SGDBR laser mirror stabilization, such as decoupling capacitors, and by reducing loop delay and increase loop bandwidth. The measured CNR was in these experiments limited by output power and receiver noise, and does not

represent the potential of the OPLL. Finally, data rate was limited by the bandwidth of the forward biased phase modulators used for data modulation. Implementing fast QCSE modulators will meet overall data performance targets. Continued efforts will be expended to improve the OPLL performance.

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APPENDIX

1. S. Ristic, A. Bhardwaj, M. J. Rodwell, L. A. Coldren, and L. A. Johansson, "Integrated Optical Phase-Locked Loop," in National Fiber Optic Engineers Conference, OSA Technical Digest (CD) (Optical Society of America, 2009), paper PDPB3.
2. S. Ristic, A. Bhardwaj, M. J. Rodwell, L. A. Coldren and L. A. Johansson, "Heterodyne Locking of an Integrated Optical Phase-Locked Loop," 2009 International Topical Meeting on Microwave Photonics (MWP'09), pp. 1-4. Oct. 2009.
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Integrated Optical Phase-Locked Loop

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Abstract: We demonstrate the first integrated optical phase-lock loop (OPLL) photonic IC, containing two SG-DBR lasers with >5 THz tuning range, a balanced detector pair and output modulators. A proof-of-concept homodyne OPLL demonstration has been performed.

OCIS codes: (250.3140) Integrated optoelectronic circuits, (060.1660) , Coherent communications (060.5060), (060.2360) Fiber optics links and subsystems.

1. Introduction

Optical phase-locked loops (OPLLs) are routinely constructed using low-linewidth solid state or external cavity lasers. They are more challenging to build using wide linewidth semiconductor lasers due to the required short feedback delay. Past semiconductor laser OPLL demonstrations have typically used miniature bulk optics to meet these latency requirements [1,2]. In this paper, we demonstrate for the first time, an integrated optical phase-lock loop photonic integrated circuit in which all required optical components are integrated, including lasers, waveguides, couplers and photodetectors, as well as optical modulators. This eliminates the latency and instability from free-space or fiber optical paths to allow a very fast and robust OPLL.

Moreover, the OPLL photonic IC is built using widely-tunable lasers with over 5 THz wavelength range. This is key to several applications. First, it allows the development of homodyne coherent receivers in the form of Costa's loop, without the requirement for complex, power hungry DSP electronics to manage laser phase noise. The relative simplicity of the Costa's loop will also allow scaling to high data rates, >100Gbps. Second, an OPLL with 5 THz wavelength tuning range will allow coherent beam forming for sub-mm resolution LIDAR applications. Third, together with a THz photodetector, it will allow optical heterodyne signal generation with a DC to 5 THz frequency range with maintained coherence. Applying optical phase or amplitude modulation to one optical line will now generate a coherent phase or amplitude modulated THz signal. This is the target application for this paper. The photonic integrated circuit is described in section 2 and a proof-of-concept homodyne OPLL demonstration is described in section 3.

2. Optical Phase Lock Loop Photonic Integrated Circuit

A diagram of the PIC is shown in Fig. 1, and the corresponding SEM image is shown in Fig. 2, left. The PIC epitaxial structure has been grown on an S-doped InP substrate by MOCVD. The integration platform used here is often referred to as "Offset Quantum Well Platform" and has been described in more detail in [3] and references therein. In this platform, the light is guided by a 300 nm 1.4Q surface-ridge-waveguide core layer, which forms a basis for "passive" components: waveguides, Multimode Interference Splitters/Couples (MMIs), and Franz-Keldysh modulators. Above this layer, the epitaxial material structure contains a 119-nm Multiple-Quantum-Well Region (MQW) region that forms a basis for "active" components: gain sections in SGDBR lasers, SOAs, as well as photodetectors. The "active" MQW region is defined by wet etching, as the very first processing step, followed by grating patterning/etching, waveguide p-cladding re-growth, and the rest of the steps, main of which are: surface-ridge wet etching, top N-contact wet etching and deposition, BCB patterning for modulators and detectors, P-metal pads, P-metal via etching, P-metal deposition, wafer thinning, and back-side N-metal deposition.

Light from each of the two SGDBR lasers is first divided by a 90-µm-long 1 X 2 MMI splitter into two equal-power components, and all four components are amplified by four 400-µm-long SOAs. One of these two components from either laser is used for the feedback loop, and the other is used for the PIC output. The half-power component from either laser that is used in the feedback loop first enters a 340-µm-long 2 X 2 MMI coupler (with tuning pads), which is, in turn, followed by a balanced receiver, containing two 250-µm-long phase modulators. These phase modulators are followed by a pair of 50-µm-long active photodetectors that can be used as a balanced receiver. The residual light that is not absorbed in the photodetectors will additionally be absorbed in 200-µm-long curved (7˚) active sections with grounded pads. The P-metal electrodes for both types of detectors are supported by

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BCB and are connected to 100 µm X 100 µm RF pads, which are laid out in a G-S-G-S-G-S-G configuration (150 µm pitch) on either side of the PIC for direct probing.

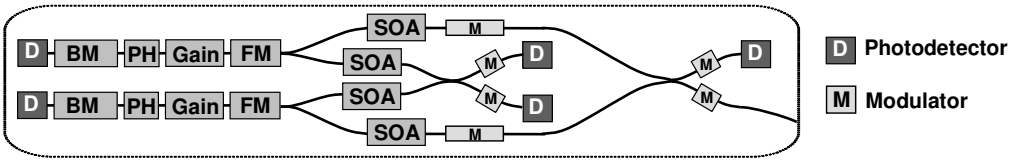

Fig.1. Functional schematic of chip.

Each of the other two half-power components from the 1 X 2 MMI splitter (directed toward the output) is first passed through a 400-µm-long phase modulator before entering a 340-µm-long 2 X 2 MMI coupler (with tuning pads). These two modulators connect to the same RF pads as the photodetectors mentioned above. Following the 2 X 2 MMI coupler, light passes through a 250-µm-long additional amplitude modulators in each branch that can be used for electronic monitoring of the PIC's output. Similar to the feedback loop, one of the modulators is followed by a photodetector (also for electronic monitoring of the output), while the other is followed by a 7˚ curved output waveguide with AR coated facet. The back sides of the SG-DBR lasers are also AR coated. The output modulators connect to RF pads that are identical to those in the feedback loop. Total length of the PIC is about 6.6 mm and its width is about 450 µm.

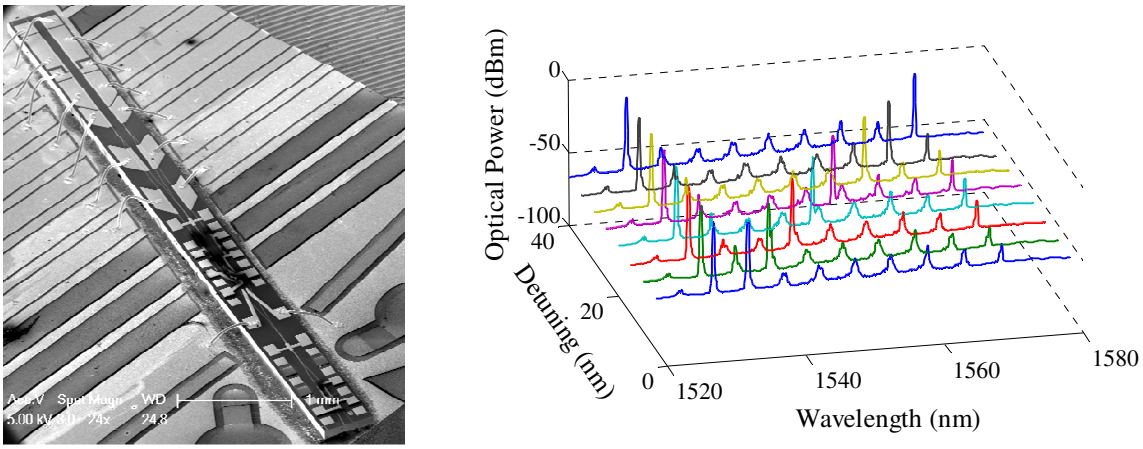

Fig.2. Left) SEM of Integrated OPLL PIC. Right) Output spectra from heterodyne optical source.

The SG-DBR lasers have more than 40nm wavelength quasi-continuous tuning range. By keeping one laser at fixed frequency and tuning the second laser, a heterodyne optical output signal is generated from the photonic IC where the heterodyne difference frequency can be selected over the full 0 to 5 THz frequency range, corresponding to the 40nm tuning range. This is illustrated by Fig. 2, right, where a series of optical spectra are captured to illustrate the output frequency range.

3. Proof-of-Concept OPLL Demonstration

A simplified schematic of the proof-of-concept OPLL arrangement is shown in Fig. 3, left. One of the integrated photodetectors is used to detect the beat signal between the two SG-DBR lasers. The detected photocurrent is then used to generate the wavelength tuning current applied to the phase section of one of the SG-DBR lasers, now acting as a current-controlled oscillator. A FET-transistor is required to translate the reverse biased detector current, to a forward biased phase section injection current. The detector load is tailored to generate a second order loop transfer function with lag compensation. In addition, the phase section is terminated by an inductor to compensate for the 3-dB bandwidth of the FM response of the SG-DBR laser (around 100MHz). The resulting loop bandwidth is around 300MHz. The free-running heterodyne beat signal is shown in Fig. 3, center, on a linear amplitude scale. The FWHM of the beat signal is around 300 MHz. However, it has been shown that the linewidth of SG-DBR lasers is dominated by low-frequency jitter [4], and as such, the phase noise can be well suppressed by a 300MHz loop bandwidth, as evidenced by the results below.

By splitting off part of the output of each laser before heterodyne detection, the phase and amplitude of each locked laser can be individually controlled. The two laser signals are then combined a second time, but now the heterodyne beat signal will carry any applied phase or amplitude modulation. In other words, this source has the potential to translate optical vector modulation to modulation on a coherent mmW or THz beat signal. For this homodyne OPLL demonstration, an applied phase modulation will directly result in a change in output amplitude due to coherent combination with the second laser output. This is illustrated by Fig. 3, right, where relatively pure phase modulation is applied by injecting a current into the phase modulator, resulting in a change in detected photocurrent in the on-chip monitor photodiode. This confirms successful optical phase locking of the two lasers. The finite extinction is a result of imbalanced detected power from the two lasers. In contrast, changing the modulator phase when the OPLL is unlocked, results only in the observation of residual amplitude modulation of the phase modulator, as also seen in Fig. 3, right.

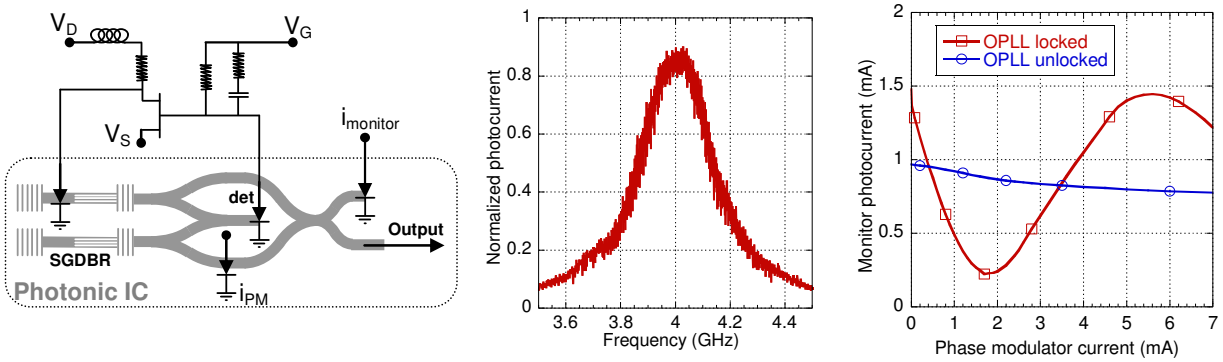

Fig.3. Left) Schematic of proof-of-concept OPLL demo. Center) Free-running laser heterodyne signal. Right) Interference between two locked lasers

4. Conclusion

In this paper we have demonstrated a monolithically integrated optical phase-locked loop photonic circuit in which all required optical components are integrated, including lasers, waveguides, couplers and photodetectors. This device includes widely tunable lasers with 5 THz tuning range and a capacity to apply modulation to a single optical line, translating optical vector modulation to a optical heterodyne signal. A simple proof-of-concept homodyne OPLL demonstration has been performed, confirming the suitability of SG-DBR lasers as a VCO laser in an OPLL. Future mmW heterodyne OPLL versions will fully utilize balanced detection, already in place on the photonic IC and integrated feedback electronics to increase the loop bandwidth and reduce laser amplitude noise fed back into the loop, for lower resulting phase noise.

Acknowledgements

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Heterodyne Locking of an Integrated Optical Phase-Locked Loop

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***Abstract*—We demonstrate proof-of-concept heterodyne locking of the first optical phase-locked loop photonic integrated circuit. The circuit contains two sampled-grating distributed reflector lasers monolithically integrated with optical amplifiers, multimode interference splitters/couplers, and high-speed modulators and photodetectors.**

I. Introduction

An optical phase-locked loop (OPLL) is a control system that exhibits both essential similarities and fundamental differences when compared to its RF counterpart. In an RF phase-locked loop (PLL), a mixer is used to detect a phase difference between an input signal and an output of a local voltage-controlled oscillator (VCO). The mixer produces a phase error signal that is filtered and applied to the VCO, tuning its output frequency to have a fixed phase relation with the input signal frequency. In an OPLL, however, a photodetector detects a phase difference between an input optical signal and an output of a local current-injection tunable laser, which effectively plays a role of a current-controlled oscillator (CCO) and is a direct equivalent of the VCO [1]. The phase error signal produced by the photodetector is filtered and applied to the CCO, tuning its output frequency to have a fixed phase relation with the input optical signal frequency. This locking can be implemented in a homodyne fashion, where the frequencies of the input light and the CCO output light are the same, or in a heterodyne fashion, where these frequencies are different (also referred to as offset locking). Because in heterodyne locking the photodetector produces a beat signal at an offset frequency, the beat signal is usually down-converted by mixing with an RF reference at the same frequency in order to generate the phase error signal that tunes the CCO.

There are many applications that utilize homodyne and heterodyne locking. For example, homodyne locking provides high receiver sensitivities [2] and can be used for coherent demodulation in double-sideband suppressed carrier (DSB-SC) communications [3]. Heterodyne locking of several "slave" lasers at the same frequency, which is offset relative to a reference "master" laser's frequency, can be used to produce a high-power coherent beam combination (CBC) [4]. In addition, heterodyne locking of two lasers has been successfully demonstrated in producing coherent optical beats with frequencies in the GHz region [5]. This single-sideband source can find many applications in microwave photonics.

Unlike an RF PLL, an OPLL is not easily locked. In an RF PLL, the RF oscillator is spectrally pure, and the feedback loop bandwidth is relatively large in comparison to the frequency of the input signal. The large loop bandwidth can easily compensate for the small phase noise of the RF oscillator. In an OPLL, however, the tunable laser linewidth can be in the MHz range, and the feedback loop bandwidth is small compared to the frequency of the input signal, which is ~193 THz (1550 nm). The feedback loop bandwidth is typically smaller, and its latency is larger, compared to the RF PLL because of the large size of optical components and interconnects. Consequently, for successful locking of an OPLL, researchers have used either a very narrow linewidth lasers (kHz range) with large and slow feedback loops [6], or wide linewidth semiconductor lasers with very compact bulk optics necessary to achieve small loop latencies [5], [7].

Recently, we have demonstrated homodyne locking of the first OPLL photonic integrated circuit (OPLL-PIC) [8]. The OPLL-PIC is monolithically integrated, and its compactness allows the use of wide linewidth tunable semiconductor lasers. The small OPLL-PIC is robust and provides for easy packaging. In this work, we demonstrate proof-of-concept heterodyne locking the OPLL-PIC.

II. An Optical Phase-Locked Loop Photonic Integrated Circuit

Fig. 1 shows a schematic of an OPLL-PIC and the external feedback electronics used in the heterodyne experiment. In

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this section, we describe the OPLL-PIC. The details about the feedback loop and the heterodyne locking experiment are presented in Section III.

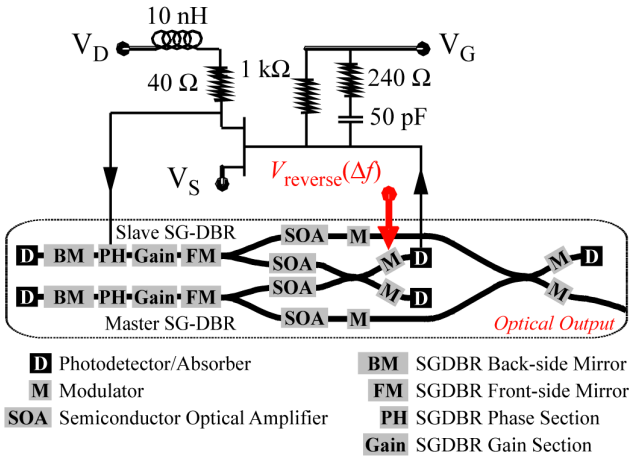

Figure 1. A schematic of the OPLL-PIC and the electronic feedback circuit used in a heterodyne locking experiment.

The monolithically integrated OPLL-PIC contains two widely tunable sampled-grating distributed reflector (SG-DBR) lasers, as well as semiconductor optical amplifiers (SOAs), multimode interference splitters/couplers (MMIs), and high-speed modulators and photodetectors. Light from each SG-DBR laser is split equally using a 90-µm-long 1x2 MMI, and each of the four output components is amplified using a 400-µm-long SOA. After amplification, the outputs from the two SG-DBR lasers are combined in two different 340-µm-long tunable 2x2 MMIs. One of the two MMIs is part of the OPLL-PIC feedback loop, and it has a 250-µm-long high-speed modulator followed by a 50-µm-long high-speed photodetector on each of its two output waveguides. The two photodetectors are used to provide the phase error signal to the feedback loop and can be used either separately or in a balanced pair configuration. The other MMI is part of the OPLL-PIC output. This MMI has a high-speed modulator on each of its two input waveguides, and similar to the feedback MMI, it also has a high-speed modulator on each of the two output waveguides. The output MMI, however, has a high-speed photodetector following a high-speed modulator only on one of its two output waveguides. This photodetector is used to monitor the coherent output beat signal in the electrical domain. The other output waveguide of the MMI is used to monitor the output beat signal from the output of the OPLL-PIC in the optical domain. The output waveguides are curved (7º) and their facets are anti-reflection coated in order to minimize reflections. The length of the OPLL-PIC is 6.6 mm, and the width is 0.45 mm. Fig. 2 shows a scanning electron microscope (SEM) image of the OPLL-PIC mounted on a carrier and wire-bonded. As can be seen in Fig. 2, there are four 100 µm x 100 µm G-S-G-S-G-S-G RF pads (150 µm pitch) used for direct probing of the high-speed modulators and photodetectors in both feedback and output sections of the OPLL-PIC.

Our monolithic integration platform is referred to as the "Offset Quantum Well Platform" [9]. The epitaxial structure is grown on a 2-inch S-doped InP wafer using Metalorganic Chemical Vapor Deposition (MOCVD). An "active" 119-nm-thick multiple-quantum-well (MQW) region that provides gain is grown on top of a "passive" 300-nm-thick 1.4Q layer. The passive layer is used to guide light as well as provide modulation either via carrier plasma effect, in the forward-bias operation of the modulator diodes and phase sections of the SG-DBR lasers, or via the Franz-Keldysh effect, in the reverse-bias operation of the modulator diodes. The active devices (SOAs, SG-DBR gain sections, and photodetectors) are defined by wet etching, after which the gratings in the back-side and front-side SG-DBR laser mirrors are defined by Electron Beam Lithography. Subsequently, the p-cladding regrowth is done, and surface-ridge waveguides are wet etched. The rest of the main fabrication steps include dry etching and deposition of top-side n-contacts (used for high-speed modulators and photodetectors), BCB patterning for high-speed modulators and photodetectors, p-contact metallization, proton implant isolation of passive waveguide sections between devices, wafer thinning, and back-side n-contact metallization (used for all of the low-speed devices).

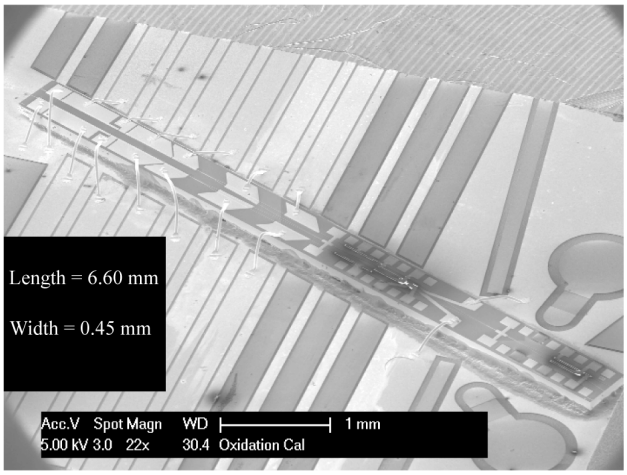

Figure 2. An SEM image of a fully fabricated OPLL-PIC after mounting on a test-carrier and wire-bonding.

III. Heterodyne Locking Demonstration

As shown in Fig. 1, in the heterodyne locking of two SG-DBR lasers, one laser plays the role of the CCO (the slave laser), and its frequency is tuned by current injection into the phase section [10]. SG-DBR lasers offer several key advantages for OPLL applications. Their tuning sensitivities are ~20 GHz/mA, and they are an order of magnitude larger than those of the semiconductor lasers typically used in OPLL applications [5]. Their large sensitivities provide large loop gains and make OPLLs more stable. In addition, SG-DBR lasers have more than 40 nm (>5 THz) of quasi-continuous wavelength tuning range. Consequently, the OPLL-PIC can generate coherent optical beams at very high frequencies and can also provide broadband wavelength operation in homodyne applications. Fig. 3 illustrates this point, where a discrete incremental detuning of one integrated, unlocked SG-

DBR laser relative to the other is plotted. Lastly, unlike distributed feedback (DFB) lasers [5], SG-DBR lasers do not exhibit phase sign inversion when tuned via current injection into the phase section. It is hard to compensate this phase inversion using feedback electronics.

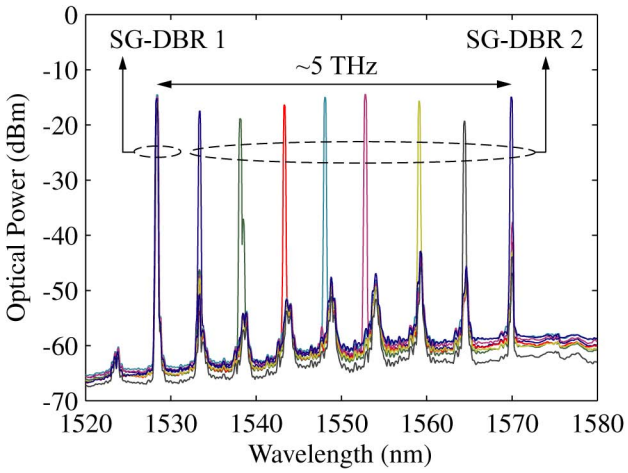

Figure 3. Optical spectra corresponding to incremental discrete detuning between the two on-chip unlocked SG-DBR lasers.

The relatively large linewidth that is characteristic of the SG-DBR laser is dominated by low-frequency jitter [11] and therefore can be well compensated by using the compact feedback loops achievable with monolithic integration. We measure linewidths of our lasers to be between 10 MHz and 50 MHz using a 30-μs-delay self-homodyne technique. Fig. 4 shows the combined linewidth of two integrated unlocked SG-DBR lasers to be ~300 MHz when measured using an external photodetector and electrical spectrum analyzer.

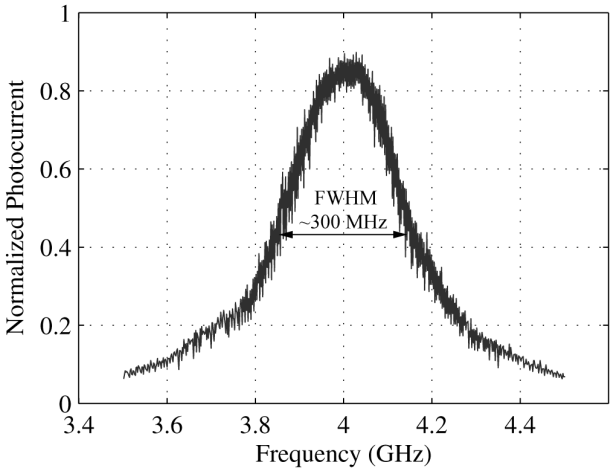

Figure 4. Combined linewidth of two unlocked integrated SG-DBR lasers.

In the heterodyne locking of the first integrated OPLL, we do not use an external mixer, which, as explained in Introduction, is a common practice [1]. Rather, for a proof-of-concept demonstration, we utilize sideband locking. In this scheme, the frequencies of the two SG-DBR lasers are detuned by the amount corresponding to the desired coherent beat frequency, *i.e.*, Δf. The combined laser outputs are then modulated with a high-speed modulator at the output of the feedback 2x2 MMI at the same frequency Δf. As shown in Fig. 1, the modulator is voltage-driven in the reverse bias regime, where the drive voltage (V_{reverse}) is applied using a microwave synthesizer. As the detuning frequency and the modulation frequencies are the same, a sideband of one laser occurs at the same frequency as the center frequency of the other laser, and sideband locking becomes possible. A phase error current signal is generated in the photodetector and provided as an input to the feedback electronic circuit, where it is amplified and filtered. Subsequently, the phase error current signal is applied to the phase section of the slave SG-DBR laser, adjusting its output frequency to have a fixed phase relation to the output frequency of the master SG-DBR laser.

A FET transistor in the feedback loop is used to amplify and adjust the polarity of the phase error current signal from the photodetector so that it can be used to drive the phase section of the slave laser. The total load seen by the feedback photodetector is designed to provide a second-order transfer function with lag compensation. The LR circuit is designed to have a zero at a frequency close to the pole in the FM frequency response of the slave laser, making it a more controllable device. The 3-dB point in the FM frequency response of the SG-DBR laser is ~70 MHZ. Since the laser itself acts as an integrator, the remaining RC circuit is required to provide only a single pole. This is achieved with the larger of the two resistors that dominates at low frequencies. The smaller resistor dominates at frequencies closer to the 3-dB point and provides a zero that is necessary to improve stability of the loop at the frequencies where the gain becomes unity. The resulting bandwidth of the loop is ~300 MHz, which, as we show below, is sufficient for locking an SG-DBR laser, in large part due to the fact that the phase noise of SG-DBR lasers is dominated by low-frequency jitter.

Figs. 5(a) and 5(b) show oscilloscope traces of the OPLL-PIC optical output before and after locking it with a 5 GHz microwave signal, which is also used to trigger the oscilloscope. Locking is achieved by gradually bringing the detuning frequency closer to the modulation frequency. As shown in Fig. 5(a), before locking, the phase noise is so large that only the envelope of the beat is observed. When the OPLL is locked, most of the power from the beat is in the locked state, as shown in Fig. 5(b). Occasional cycle slipping of the OPLL is evident in the jitter shown in Fig. 5(b). Fig. 6 shows the corresponding phase noise spectrum of a locked OPLL-PIC, measured using an external photodetector and an electrical spectrum analyzer. The phase noise reaches maxima at frequencies ~300 MHz below and above the 5 GHz offset frequency because the loop becomes unstable when operating at frequencies exceeding its bandwidth (~300 MHz).

There is a significant noise penalty associated with the sideband locking scheme because the power in the sidebands is a fraction of the power in the main lobes, producing an inefficient mixing in the photodetector. For the same reason, the modulation power needed for successful locking in our experiment is around 10 dBm. The noise penalty could be decreased by using an external RF mixer, which is a more complicated setup. In the future work, feedback electronics

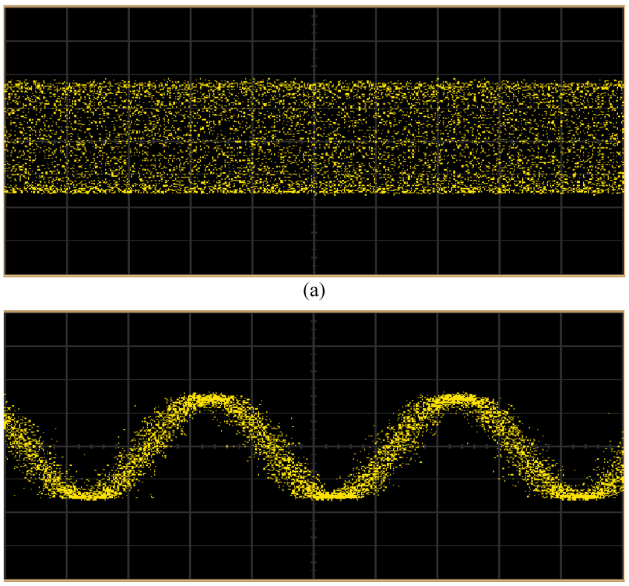

Figure 5. Oscilloscope traces of the OPLL-PIC optical output (a) before and (b) after heterodyne locking of the SG-DBR lasers at a 5GHz frequency offset. Both traces are 500 ps long.

will be integrated to further improve the loop bandwidth and decrease the phase noise. In addition, the on-chip feedback photodetectors will be used in a balanced configuration, which should decrease the phase noise penalty due to laser amplitude noise.

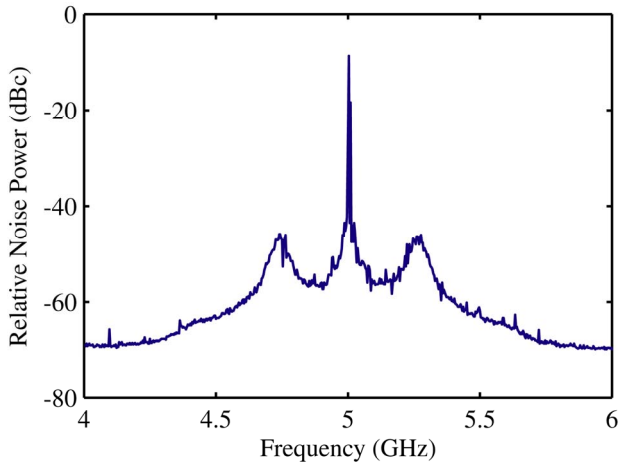

Figure 6. Phase noise spectrum of the OPLL-PIC output corresponding to heterodyne locking of the two SG-DBR lasers at a 5 GHZ frequency offset.

IV. Conclusion

In this paper, we have demonstrated a proof-of-concept heterodyne locking of the first integrated OPLL. The OPLL-PIC contains two SG-DBR lasers monolithically integrated with SOAs, MMIs, and high-speed modulator and photodetectors. The monolithic integration enables small-latency (large-bandwidth) feedback loops, necessary to compensate for wide linewidths of SG-DBR lasers, and semiconductor lasers in general. SG-DBR lasers offer large tuning sensitivities, they are well-behaved when used as CCOs, as they do not suffer from the phase inversion problem, and they offer wide wavelength tuning ranges, *i.e.*, large coherent beat frequencies. The OPLL-PIC contains on-chip modulators that can be used for modulation of a coherent millimeter-wave beat. The technology is robust, has a small footprint, and provides for easy packaging. Future improvements of the OPLL will be achieved by using both feedback detectors as a balanced receiver pair in order to reduce laser amplitude noise, which increases the phase noise of the OPLL. In addition, more sophisticated, integrated feedback electronics will be used in order to further decrease the feedback loop latency, thereby decreasing the phase noise of the OPLL.

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An Optical Phase-Locked Loop Photonic Integrated Circuit

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***Abstract*—We present the design, fabrication, and results from the first monolithically integrated optical phase-locked loop (OPLL) photonic integrated circuit (PIC) suitable for a variety of homodyne and offset phase locking applications. This InP-based PIC contains two sampled-grating distributed reflector (SG-DBR) lasers, semiconductor optical amplifiers (SOAs), phase modulators, balanced photodetectors, and multimode interference (MMI)-couplers and splitters. The SG-DBR lasers have more than 5 THz of frequency tuning range and can generate a coherent beat for a wide spectrum of frequencies. In addition, the SG-DBR lasers have large tuning sensitivities and do not exhibit any phase inversion over the frequency modulation bandwidths making them ideal for use as current controlled oscillators in feedback loops. These SG-DBR lasers have wide linewidths and require high feedback loop bandwidths in order to be used in OPLLs. This is made possible using photonic integration which provides low cost, easy to package compact loops with low feedback latency. In this paper, we present two experiments to demonstrate proof-of-concept operation of the OPLL-PIC: homodyne locking and offset locking of the SG-DBR lasers.**

***Index Terms*—Integrated optoelectronics, coherent optical communications, optical phase-locked loops, tunable semiconductor lasers.**

I. Introduction

EVER since the first demonstration of an Optical Phase-Locked Loop (OPLL) [1], a significant research effort has been invested in developing the system for a wide range of applications, as shown in [2]–[4] and references therein. In optical communications, the OPLL allows synchronous coherent receivers where mixing the received signal with a high-power local-oscillator (LO) laser provides high sensitivity and out-of-band noise suppression [5]–[7]. For carrier-suppressed modulation schemes, a Costa's loop can be used [8]. OPLLs are commonly used for optical clock recovery in digital telecommunication systems [9]. They have also been developed for generation of stable channel offsets in dense wavelength-division multiplexed (DWDM) systems [10]. In microwave photonics, an OPLL can form a microwave single-sideband optical source [2] with the potential for endless microwave phase adjustment. This is an attractive property for implementation of a phased array microwave system. OPLLs also find applications in free-space optical systems such as LIDAR systems, where they allow coherent combination of several coherent optical sources [3], potentially to form large swept optical phase arrays.

Compared to fiber lasers and solid state lasers with narrow linewidths, semiconductor lasers are generally favored because of their small sizes, low costs, and high efficiencies [2], [11]. In addition, the phase and frequency tuning of a semiconductor laser, which is necessary for the laser to be used in the negative feedback loop of an OPLL, is easily achieved by current injection. So far, the central difficulty in realizing OPLLs using semiconductor lasers has been the strict relation between laser phase noise and feedback loop bandwidth. The wide linewidths observed in semiconductor lasers, typically in the MHz range, require sufficiently wide loop bandwidths, *i.e.*, small loop delays. In the past, this has been addressed by using low-linewidth external cavity lasers that allow longer feedback loop delays [12], [13], or by construction of compact OPLLs using miniaturized bulk optical components to meet the delay restrictions arising from the use of standard semiconductor lasers [2], [14]. Other efforts include relaxing this restriction by combining an OPLL with optical injection locking, thereby gaining the wide locking bandwidth of optical injection, while a slow phase-lock loop with a long delay allows long-term stability [15].

Recent progress in device design and fabrication has enabled distributed-feedback (DFB) lasers to have sub-MHz linewidths, without external cavity linewidth reduction schemes, [3], [8], [14], [16]–[18]. Consequently, the delay in

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fiber-based OPLLs is not the bandwidth limiting factor in locking the standard DFB lasers. Rather, the loop bandwidth is limited by the phase reversal in the FM response, which is characteristic for DFB lasers and occurs at frequencies between 0.1 and 10 MHz [2], [16], [19], [21], as explained in Section III. While this lower loop bandwidth is sufficient for locking of DFB lasers even in fiber-based OPLLs, it is still a limiting factor in achieving high-performance OPLLs with very small phase errors because the benefits of locking are constrained to the narrow bandwidth determined by the phase reversal [2], [11], [16]. In the applications such as the coherent beam combining [16], where several lasers are locked, the cumulative phase error increases with the number of lasers, and it is important to minimize it.

In order to overcome the phase-inversion-limited FM bandwidth of standard narrow-linewidth DFB lasers, new types of semiconductor lasers have been developed for their use in OPLLs. Complex-coupled DFB lasers have been shown to have flat FM responses without phase inversion between 10 KHz and over 20 GHz [22]. The requirement for precise control of the lasers' bias current and the fact that the FM-response uniformity and sensitivity depend on the output power level are disadvantageous for OPLL applications [19]. Multi-section tunable semiconductor lasers have been very popular in the past in OPLLs [2], [17], [19], [23], [25]. Here, the phase tuning section is separated from the gain section and the Bragg section, which minimizes the thermal tuning issues responsible for the phase inversion in DFB lasers.

Integration of an OPLL is considered to be beneficial for a wide range of applications by researchers in the field [2], [3], [10], [13], [14], [17], [25]. Monolithic integration of the optical components in an OPLL can improve its robustness to temperature and environmental variations, which can be detrimental in fiber-based systems [16]. These variations have smaller cumulative effects on light when it propagates through a robust and compact, monolithically integrated optical components. In addition, the whole photonics integrated circuit (PIC) that includes the semiconductor lasers and the optical components of the OPLL can be maintained at a constant temperature by the same temperature controller. Typical integrated optical waveguides and devices preserve the polarization of light, so that no polarization alignment between the components is necessary in order to maximize the interference between the integrated lasers in the applications where multiple lasers are being locked. Furthermore, integrated waveguides are immune to long term polarization drifts. Also, compared to the miniature bulk optics OPLLs [2], no alignment between the components needs to be performed. The compactness and ease of packaging of integrated OPLLs can improve their cost effectiveness. This is especially true for the applications where multiple lasers are locked together [3], [11], [26].

Monolithic integration of multi-section lasers is strongly motivated by two factors. First, in multi-section lasers the passive phase and Bragg sections are already integrated with the active gain section. In order to achieve this, a regrowth or some other type of post-growth bandgap engineering technique, such as quantum-well intermixing, is necessary [27], thereby facilitating integration of additional active devices, such as semiconductor optical amplifiers (SOAs) and photodetectors, and passive devices, such as modulators and multimode interference (MMI) couplers and splitters. Second, compared to DFB lasers, multi-section lasers have larger linewidths, in the several-MHZ range. Although, a state-of-the-art OPLL performance has been achieved with multi-section lasers and miniature bulk optics [2], monolithic integration can offer further performance improvement by reduction of the loop delay. Monolithic integration can also enable a variety of other types of wide-linewidth lasers to be used in OPLL applications, such as widely-tunable Sampled Grating Distributed Feedback (SG-DBR) lasers.

So far, monolithic integration has focused on the receivers and on the electronic components rather than the optical components of an OPLL [10], [28], [29]. In this paper, we demonstrate for the first time, an OPLL photonic integrated circuit (OPLL-PIC) in which all required optical components are monolithically integrated, including: lasers, passive optical waveguides, MMI couplers/splitters, high-speed photodetectors, and high-speed optical phase modulators. Moreover, the OPLL-PIC uses widely-tunable SG-DBR lasers that have a wavelength tuning range greater than 5 THz [30]. This is a key feature for several applications. First, it allows the development of homodyne coherent receivers in the form of Costa's loop, with an optical bandwidth exceeding the entire C-band. The relative simplicity of the Costa's loop also allows scaling to high data rates, exceeding 100Gbps. Second, an OPLL with 5 THz wavelength tuning range can be used for coherent beam forming for sub-mm resolution LIDAR applications. Third, together with a THz photodetector and electronics, it allows optical heterodyne signal generation with a DC to 5 THz frequency range. Applying optical phase or amplitude modulation to one optical line can be used to generate a coherent phase or amplitude modulated THz signal. The rest of the paper is organized as follows: the design and fabrication of the OPLL-PIC is described in Section II, the SG-DBR laser performance is described in Section III, proof-of-concept homodyne and offset locking OPLL demonstrations are presented in Section IV, and the conclusion remarks are presented in Section V.

II. Optical Phase-Locked Loop Photonic Integrated Circuit

A. OPLL Basics

An OPLL has both parallels and fundamental differences when compared to its RF equivalents. In a microwave loop, it is a voltage-controlled oscillator that typically tracks the input signal. In an OPLL, wavelength tuning of a laser takes this role, achieved typically by current injection [3]. An RF phase-locked loop (PLL) can be built using spectrally pure

oscillators, which allow stable operation in a narrowband loop to enable filtering, or it can be built using compact integrated circuits to have a substantial fractional loop bandwidth compared to the carrier frequency, allowing agile tracking of a frequency modulated signal. In contrast, an OPLL is built using less compact optical components, leading to a smaller loop bandwidth, and with a carrier frequency of ~193THz (1550nm), which results in low loop bandwidth to carrier frequency ratio. As a result, acquiring locking is less straightforward in an OPLL as the slave laser must be tuned to the master laser wavelength with high accuracy.

Fig. 1 shows a simple schematic of the OPLL architecture demonstrated in this paper. Two widely tunable SG-DBR

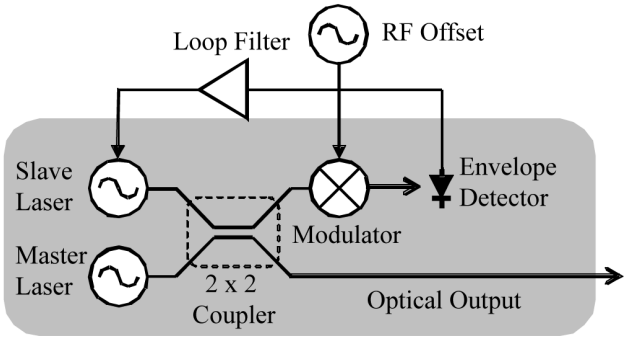


Fig. 1. Schematic of an OPLL heterodyne offset locking experiment.

lasers are monolithically integrated on a single InP substrate along with all of the other optical components needed to form the OPLL. One laser takes the role of a master laser, while the other takes the role of a slave laser. The outputs of the two lasers are first combined using a 2x2 optical coupler. The combined beat signal is then amplitude modulated for offset-locking using an integrated optical modulator and envelope-detected using an integrated photodetector. The current output from the photodetector is filtered and fed back into the salve laser. The resulting slave laser frequency tuning is then given by

$$\frac{d\varphi_s}{dt} = h_m * h_d * f_{LF} * h_s * \left(2R\sqrt{mP_mP_s}\sin(\varphi_m - \varphi_s)\right), \quad (1)$$

where the terms in the convolution: h_m, h_d, f_{LF}, and h_s are the impulse response of modulator, detector, loop filter and slave laser frequency tuning, respectively. R is the detector responsivity, P_m and P_s are the master and slave laser powers incident on the photodetector, and φ_m and φ_s are the phases of the master and slave laser respectively. Also, m is the relative power of the modulation sidebands used for offset locking after optical modulation. For zero offset locking, *i.e.*, homodyne locking, no optical modulation needs to be applied and $m = 1$. Assuming locked condition and small phase error ($\varphi_m \approx \varphi_s$), the equation can be linearized ($\sin(x) \approx x$) and the Laplace transform applied:

$$\varphi_s = \frac{H_m H_d F_{LF} H_s 2R\sqrt{mP_mP_s}}{s}(\varphi_m - \varphi_s) = G(s)(\varphi_m - \varphi_s). \quad (2)$$

Here, $G(s)$ is the open-loop gain function from which stability and operation of the loop can be evaluated. It is interesting to note that offset locking of our OPLL could also be achieved without the on-chip modulation of the two laser outputs, but rather by mixing the photodetector current with an external RF reference. In our method, the generated sidebands carry only a fraction of power of the laser outputs and thus produce small interference extinction ratios when mixed together, incurring additional noise penalty. The advantage is that no RF electronics is required.

B. OPLL-PIC Design

Figs. 2(a) and 2(b) show schematics of our two different OPLL-PIC designs. The design shown in Fig. 2(a) is intended for locking of an on-chip tunable laser to an external laser, while the design shown in Fig. 2(b) is intended for offset locking of two on-chip tunable lasers. Each OPLL-PIC design comprises of three sections that are labeled in Figs. 2(a) and 2(b) as: Laser Section, Middle Section, and Output Section. We choose the SG-DBR laser because of its wide tuning range, large frequency-modulation (FM) tuning sensitivity, and absence of phase inversion in the frequency response, as explained in Section III.

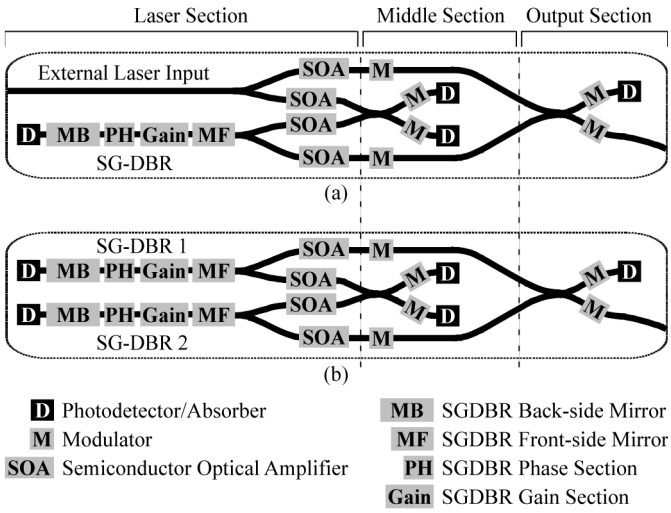


Fig. 2. Schematic of (a) an OPLL-PIC for locking to an external laser and (b) an OPLL-PIC for offset locking of two on-chip lasers.

In Figs. 2(a) and 2(b), we explicitly show the constituent components of the SG-DBR laser: front-side mirror (MF), gain section, phase section (PH), back-side mirror (MB), and back-side absorber/photodetector (D). Light from each laser is first split using 1x2 MMIs into two half-power components. One of the two half-power components from each laser is directed into a 2x2 MMI, which is a part of the feedback loop, and which is located in the Middle Section of the OPLL-PIC. The remaining half-power component from each laser is directed into a 2x2 MMI in the Output Section of the OPLL-PIC. Each of the four half-power optical paths has an SOA to adjust the optical power in each path. Each optical path at the output of the 2x2MMI coupler in the middle section of the OPLL-PIC contains a phase modulator (M), followed by a photodetector

(D), which can be used in a balanced receiver configuration. Similarly, each optical path at the two outputs of the 2x2 MMI in the Output Section of the OPLL-PIC contains a phase modulator. One of these two output waveguides ends upon a photodetector that can be used for electrical-domain monitoring of the interference resulting from the beating of the two lasers. The other output waveguide extends to the edge of the OPLL-PIC to enable coupling into an optical fiber and can be used for optical-domain beat monitoring. The 2x2 MMI in the Output Section has phase modulators on its input waveguides as well, which can be used for additional phase control.

Fig. 3(a) shows a Scanning Electron Microscope (SEM) image of an OPLL-PIC based on the schematic shown in Figure 2(b), which enables offset locking, after it has been mounted on a carrier and wire-bonded. The distinct OPLL-PIC sections mentioned above are marked for identification. The OPLL-PIC is 6.6 mm long and 0.45 mm wide.

The Laser Section of the OPLL-PIC is shown in greater detail in Fig. 3(b). The abbreviations used in labeling the various components of this section are explained in Fig. 2. This section also includes the two 1x2 MMI splitters and the four SOAs. As shown in Fig. 2, there are four SOAs in the PIC, one on each output of both 1x2 MMI splitters. Some variations of the PIC, approximately one third of the devices, were designed to have only two SOAs, one for each laser, placed at inputs of the 1x2 MMI splitters. Although additional biasing is required, the advantage of having four SOAs at the outputs of the 1x2 MMI splitters is that they can be used to equalize the lasers' output powers for better, more efficient interference. In this work, however, due to the test bench limitations, the SOAs were wirebonded together to the same pad on the carrier.

Fig. 3(c) shows the Middle Section of the OPLL-PIC. The 2x2 MMI in this section can be tuned by current injection [31], [32], although we have not done it in this work. The modulator and photodetector at the output of the 2x2 MMI connect to RF pads that are arranged in a G-S-G-S-G-S-G configuration for direct probing, with 150 µm pitch and 100 µm x 100 µm surface area per pad. Two 200 µm long curved (7˚) active sections with grounded pads, absorb light that is not absorbed in the two photodetectors.

Fig. 3(d) shows the Output Section of the OPLL-PIC. The two modulators and the photodetector at the outputs of the 2x2 MMI connect to RF pads that are arranged in the same way as those in the Middle Section of the OPLL-PIC, except that here there are three unused pads. The output waveguides that enable coupling into an optical fiber are angled at 7˚ with respect to the direction normal to the cleaved facet, and anti-reflection coatings are applied in order to minimize facet reflections.

C. *OPLL-PIC Fabrication*

For monolithic integration of the SG-DBR lasers with the other components of the OPLL-PIC, an integration platform that is often referred to as "Offset Quantum Well (OQW)"[51]

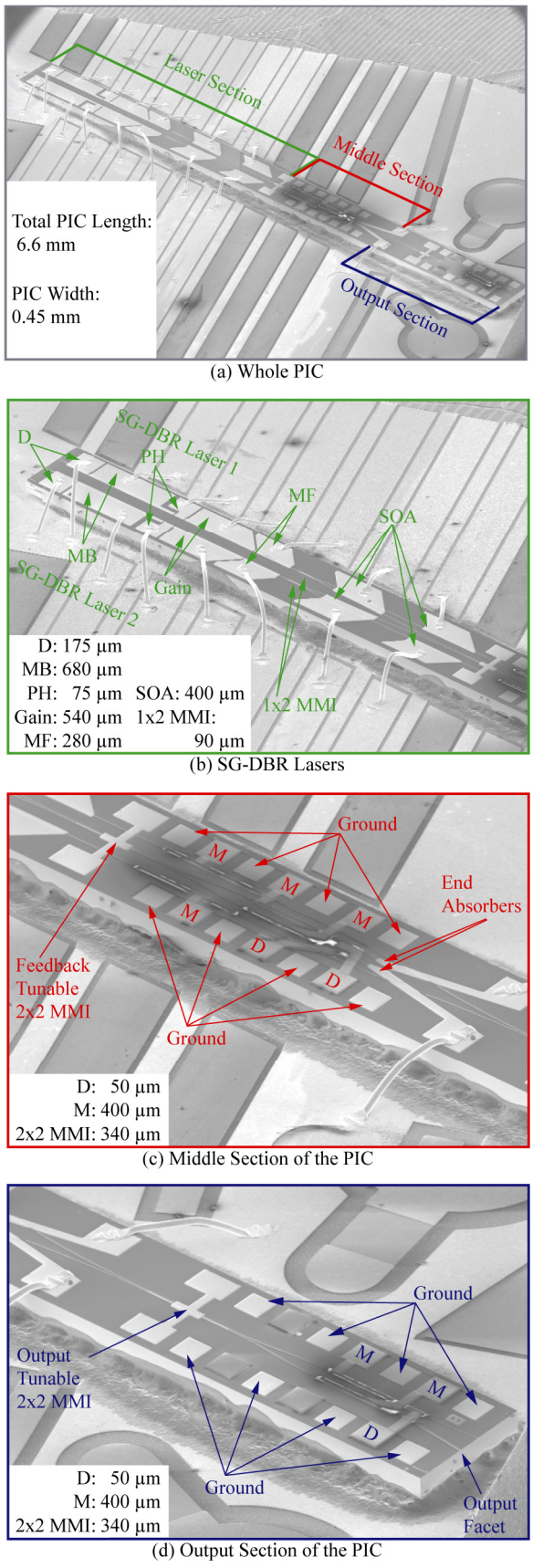


Fig. 3. SEM images of the OPLL-PIC and its various sections.

Platform [27] is used. In this platform, light is guided by a "passive" 1.4Q bulk layer that forms a basis for waveguiding, as well as modulation through current injection [33] or the Franz-Keldysh effect if reverse biased [34]. Above this layer, light couples evanescently to an "active" multiple-quantum-well (MQW) layered structure that is present only in the regions that form SOAs, gain sections of SG-DBR lasers, and photodetectors [27].

Fig. 4 shows details of the base epitaxial layer structure used in the OQW platform that is grown on a 2-inch S-doped InP wafer by Metal-Organic Chemical Vapor Deposition (MOCVD). A 2 µm thick Si-graded-doped InP buffer is grown on the substrate to reduce the overlap of the optical mode confined to the 1.4Q waveguiding layer with the heavily doped substrate and minimize the free-carrier-induced optical propagation loss in the waveguide. The buffer doping is graded from ~1e19 cm^{-3}, close to the substrate, to ~1e18 cm^{-3}, close to the 1.4Q waveguide core layer. A 300 nm thick, unintentionally doped (UID), 1.4Q waveguiding layer is epitaxially grown over the graded InP buffer, followed by a 20 nm thick 1.2Q separate confinement heterostructure (SCH) layer, a 10 nm thick InP etch-stop layer, an active region comprised of Multiple Quantum Wells (MQW) layers with a total thickness of 119 nm, another 30 nm thick 1.2Q SCH layer, a 60 nm thick UID InP spacer, and a 150 nm thick Zn-doped (1e18 cm^{-3}) InP cap. The thin InP spacer underneath the Zn-doped InP cap helps prevent diffusion of Zn dopant into the active MQW layer, and the Zn doping in the InP cap helps in controlling the position of the p-i-n junction formed after regrowth. The Photoluminescence peak of the active MQW layers was measured to be ~1560 nm.

	150 nm InP, Zn (1e18 cm^{-3})
	60 nm InP, UID
	30 nm 1.2Q, UID
"active layer"	119 nm MQW, UID
	10 nm InP, UID
	20 nm 1.2Q, UID
"passive layer"	300 nm 1.4Q
	2000 nm InP, graded Si-doped
	S-doped InP substrate

Fig. 4. "Offset Quantum Well" base epitaxial structure.

The 2-inch wafer is cleaved into four different quarters and each quarter is processed separately. In Fig. 5(a)-(e), we illustrate the processing steps used in the fabrication of the OPLL-PIC. Starting from the base epitaxial structure shown again in Fig. 5(a), Fig. 5(b) illustrates the active/passive wet etch step, where the "active" regions are etched away everywhere on the wafer except in the areas that define the

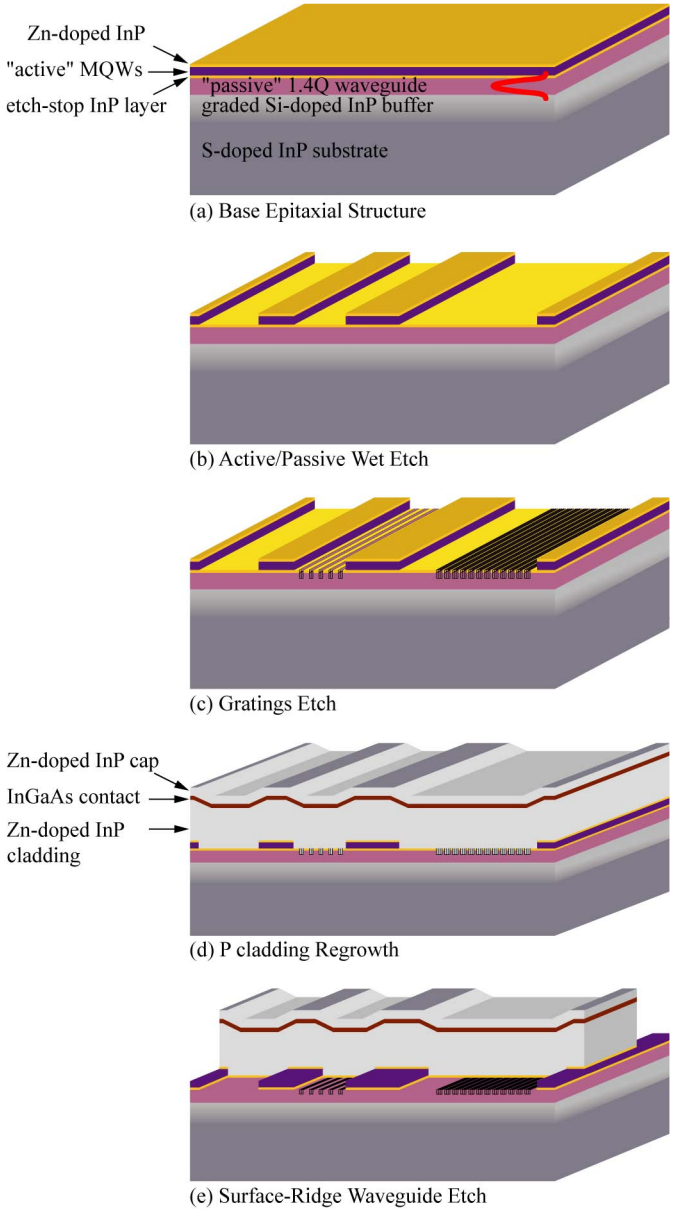


Fig. 5. "Offset Quantum Well Platform": schematics of the main processing steps starting with the base epitaxial structure.

SOAs, gain sections of the SG-DBR lasers and the photodetectors. A 100 nm thick Silicon Nitride (SiN_x) layer is deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD), and 5× Stepper Lithography is used to define the active regions by patterning photoresist that is spun on top of the SiN_x layer. All SiN_x depositions in this work are done at 250 ºC. The pattern is transferred to SiN_x by CF_4/O_2-based Reactive Ion Etching (RIE). The SiN_x hard mask protects the InP cap, spacer layers at the top of the wafer, and the active MQW and SCH regions during wet etching steps that selectively remove these layers elsewhere. The SiN_x mask is subsequently removed using Buffered Hydrofluoric Acid (BHF).

The gratings in the SG-DBR sections are defined in the passive 1.4Q layer using a Methane/Hydrogen/Argon (MHA)-based RIE, as shown in Fig. 5(c). The targeted grating depth is

around 100 nm and duty cycle is 50%. The gratings are patterned onto a high-resolution photoresist using Electron-Beam Lithography. The grating pattern is transferred to a 50 nm thick SiO_2 layer using CHF_3-based RIE, which, in turn, is used as a hard-mask for the MHA RIE step that etches the grating into the 1.4Q layer. The grating period is targeted to be ~240 nm so that the center wavelength of the SG-DBR laser is close to 1550 nm. The sampled gratings are used in both the front-side and back-side mirrors of the SG-DBR lasers. The front-side mirror consists of 5 grating bursts, each burst being 6 μm long, that repeat periodically with an interval of 61.5 μm. The back-side mirror consists of 12 grating bursts, each burst being 4 μm long, that repeat periodically with an interval of 68.5 μm. More details about the wide wavelength tuning using the Vernier effect achievable with SG-DBR lasers can be found in [35]. The SiO_2 layer is subsequently removed using BHF, and the sample is thoroughly cleaned in UV-ozone prior to the regrowth step.

This is followed by a regrowth step, as shown in Fig. 5(d). The regrowth layers comprise of a 50 nm thick UID InP spacer that helps prevent diffusion of Zn from p-doped cladding into the underlying MQW layers in the active regions and the 1.4Q layer in the passive regions of the OPLL-PIC, a 2000 nm of Zn-doped InP cladding, where the doping is 7e17 cm^{-3} in the lower half of the cladding and 1e18 cm^{-3} in the upper half of the cladding, a 100 nm thick Zn-doped (1e19 cm^{-3}) InGaAs contact layer followed by a 200 nm thick Zn-doped (1e18 cm^{-3}) sacrificial InP cap layer, on the top of the wafer, which is used to protect the thin InGaAs contact layer during the processing steps prior to metallization. The p-doping in the InP cladding layer is decreased closer to the waveguide core in order to reduce the free-carrier-induced optical loss.

Following the regrowth, surface-ridge waveguides are etched, as shown in Fig. 5(e). First, an MHA-based RIE using a 100 nm thick SiN_x hard mask is used to etch the waveguides to a depth of ~1.5 μm below the regrown InGaAs layer. Following the dry etch, the surface ridge waveguide is further etched by a $HCl:H_3PO_4$ wet etch cleanup so that the rest of the p-doped InP cladding is removed. The 1.2Q layers directly above the MQW layer in the active regions and directly above the 1.4Q layer in the passive regions act as etch-stops for the selective wet-etch. All waveguides deviate less than 7˚ from the normal to the major plane, so that minimal undercutting of waveguide walls is observed. In one quarter of the fabricated PICs, including the PIC presented in this paper, waveguides widths are adiabatically tapered from 3 μm, starting at the outputs of the 1x2 MMI splitters to 2 μm at the input of the feedback loop 2x2 MMI coupler. This is done over a distance longer than 300 μm in order to minimize the radiation losses. Similar tapering is done for the waveguide sections entering the output 2x2 MMI coupler. Since our passive waveguides are weakly multimoding when they are 3 μm wide, the tapering is used to diminish the negative effect that multimoding has on the extinction ratio of interference of the two lasers' outputs in the 2x2 MMI coupler. As the wider waveguide sections have lower loss, outputs of the 2x2 MMI couplers are tapered back to 3 μm in a similar manner. Passive waveguide widths in the rest three quarters of the PICs are maintained at 3 μm. By comparing PICs with tapered waveguides to those with non-tapered waveguides, the effect of weak multimoding on the extinction ratio can be studied. Waveguide sections for input and output coupling of light are curved by 7˚ and their widths are tapered to 5.5 μm in order to minimize facet reflections. In addition, anti-reflection coatings are applied to the facets after the processing steps are completed. Together with the 7˚ waveguide curves and the 5.5-μm tapers, total facet reflectivity of less than 10^{-4} is expected, which has been shown to be necessary for similar PICs [36], [37].

The processing steps that follow the ridge waveguide etching are fairly common and not necessarily characteristic of our integration platform. Here, we summarize the remaining steps. Fig. 6, shows various sections of the OPLL-PIC after these processing steps have been completed.

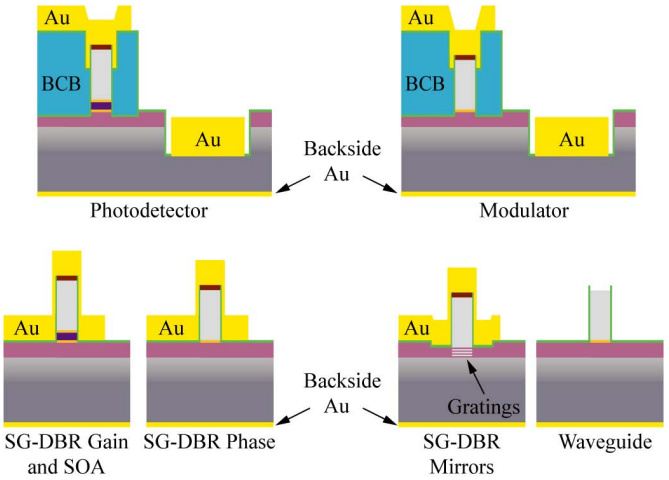


Fig. 6. Schematics showing cross sections of various components of the fully processed OPLL-PIC.

First, a thick photoresist is pattered so that it covers the entire sample except ~12 μm on each side of the ridge waveguides sections that form the high-speed modulators and high-speed photodetectors. The waveguides are still protected by SiN_x hard mask that was used to etch the surface ridges in the previous step. MHA-based RIE is used to remove the top 20 nm thick 1.2Q SCH layer and approximately 80 nm of the underlying 1.4Q layer. Both of these layers contain Zn atoms that diffuse from the p-doped InP cladding during regrowth. These Zn atoms can considerably increase the capacitance for the detectors and modulators, necessating the dry etching of the top 100 nm of the quaternary semiconductor.

An additional 100 nm thick SiN_x layer is deposited and patterned to provide a hard mask for MHA-based RIE that is used to etch windows for top N-contact metallization. The etch is performed until it penetrates ~0.5 μm below the Si-graded-doped InP buffer into the heavily doped substrate. A thick photoresist covers the wafer everywhere except the N-contact

metallization window regions. An electron-beam evaporator is used to deposit a Ni/AuGe/Ni/Au contact, which is patterned using the lift-off technique. The thickness of gold deposited during this step is only ~0.5 μm as more gold is added during the P-contact metallization step. As illustrated in Fig. 6, the top N-contact is made only for fast devices, *i.e.*, photodetectors and modulators. Top N-contacts are typically required for the PICs that are fabricated on semi-insulating substrates to provide low-loss connection to the ground plane [32], [36]. The main reason for having the top N-contacts in our proof-of-concept demonstration is the ease of direct RF probing, as discussed in Section II B. N-contact for the remaining devices is achieved by back-side metallization at the end of processing. The N-contacts are annealed at 430 ºC for 30 s. After the top N-contact metallization, a thin SiN_x layer is deposit and photo-sensitive BCB is spun, developed, and cured at 250 ºC. This leaves BCB in places that will be underneath the P-contact metal pads and traces running along the lengths of the high-speed photodetectors and modulators and covering the surface ridges in these regions. Along with the capacitance reduction etch, the BCB further reduces the capacitance of these devices to the extent that should enable their operation at frequencies far exceeding 10 GHz. The P-metal pads without BCB are separated from the top surface of the wafer (1.2Q stop-etch layer) by sub-micron-thick SiN_x. BCB is used to elevate the P-metal pads farther from this surface, and thus farther from the N-doped substrate, so that this increased separation combined with the small dielectric constant of BCB (2.65), provide lower capacitance compared to the P-metal pads without BCB [36]. An additional thin SiN_x layer is deposit after BCB patterning. Thus, the BCB is sandwiched between thin layers of SiN_x, shown as thin green lines in Fig. 6, for better adhesion to the semiconductor surface below as well as the P-contact metal on top.

Three different types of P-contact metal vias need to be opened in the top SiN_x layer prior to the P-contact metallization. First, vias are formed by removing the SiN_x layer above N-contact metal. This is accomplished by patterning photoresist to cover the sample everywhere except over the N-contact metal and dry etching the SiN_x layer above the N-contact metal using CF_4/O_2-based RIE. The next via is formed by removing the SiN_x layer on top of all the ridge waveguide sections except those covered with BCB. To open this via, photoresist is partly developed around the waveguides and partially etched back using O_2-based RIE until the ridge tops are exposed. CF_4/O_2-based RIE is then used to etch the SiN_x layer and expose the InP cap layer that is on top of the ridge waveguides. The remaining SiN_x on the sidewalls of the ridge and over the rest of the wafer is protected by photoresist during this step. Finally, vias through the BCB layers are opened using a two-step process. A 5-μm-wide via is etched using CF_4/O_2-based RIE to expose the ridge top buried underneath 3.7-μm-thick BCB and the SiN_x layers. This etch needs to be timed in order to minimize the difference in height between the ridge top and the BCB, and, consequently, minimize the P-contact capacitance. SiN_x is then re-deposited to fill in any openings that typically develop between the waveguide sidewalls and BCB, and a new via that is narrower than the waveguide is dry etched until the BCB and SiN_x layers are completely removed thereby exposing the InP on the top of the ridge.

At this point the sacrificial InP cap layer is removed using $HCl:H_3PO_4$-based wet etch everywhere along the ridge waveguides, thus exposing the InGaAs contact layer.

Standard Ti/Pt/Au 8-μm-wide P-contact metal is deposited by electron-beam evaporation, where gold thickness is over 2 μm. During the deposition, the sample is mounted to a rotation stage tilted at ~30º for maximum sidewall coverage. The P-contact metal is patterned using the lift-off technique. The thermal annealing is done at 400 ºC for 30s.

After the P-contact metallization is completed, the passive waveguide sections that are not covered by metal are further processed. At this point, the SiN_x layers and the sacrificial InP cap layer are missing from the top surfaces of these waveguide sections, and the InGaAs contact layer is exposed. A thick photoresist is first patterned so that it covers the entire sample, including the metalized waveguide sections, except ~12 μm on each side of the passive waveguide sections. The top InGaAs contact layer is then removed from the ridge tops in these sections using a $H_3PO_4:H_2O_2:H_2O$-based selective wet etch. SiN_x layers protect the top 1.4Q layer on each side of the ridge during this etch step. The same photoresist mask is subsequently re-patterned, and the wafer quarter is subjected to proton implantation. Proton implantation along with the removal of the InGaAs contact layer increase the electrical isolation between neighboring devices and reduces the free-carrier-induced optical loss. The use of proton implantation for neutralizing Zn acceptors, which dominate the carrier-induced loss, is described in [38]. Typical passive waveguide loss for our integration platform is ~2.5 dB/mm [37].

The wafer quarter is then thinned to a thickness of ~130 μm, for the ease of cleaving. Back-side Ti/Pt/Au metallization is performed using electron-beam evaporation, where the thickness of gold is around 0.3 μm. The thermal annealing is done at 380 ºC for 30s. The sample is cleaved into bars along facets that have the waveguides for input or output coupling to an optical fiber. Anti-reflection coatings are applied to these facets to further reduce reflections. Individual devices are then cleaved and mounted on carriers and wire-bonded.

III. SG-DBR Laser Performance

Besides the fact that it is a well established technology, there are at least four important characteristics of the SG-DBR laser that make it a very attractive choice for its use in an OPLL.

First, SG-DBR lasers have in excess of 40 nm of quasi-continuous wavelength tuning range, as shown in the optical spectrum analyzer spectra plotted in Fig. 7. In this figure, one of two on-chip SG-DBR lasers is tuned to a constant

wavelength, while the wavelength of the other on-chip SG-DBR laser is detuned away from that wavelength in increments of ~5 nm. This wide wavelength tuning range enables the OPLL-PIC to generate a heterodyne beat frequency that spans from DC to over 5 THz.

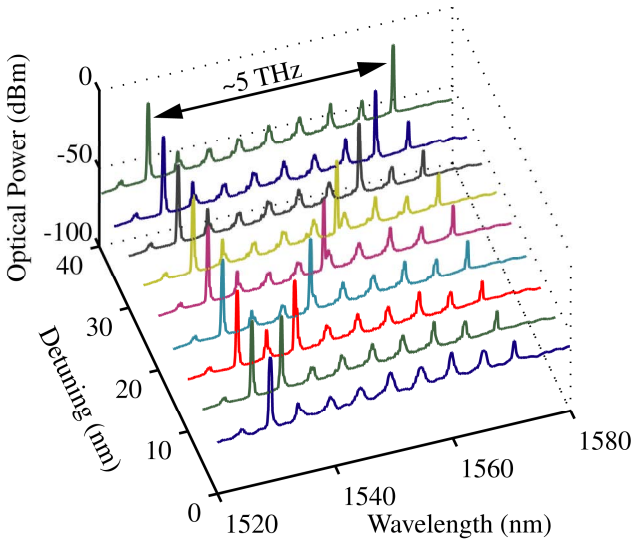


Fig. 7. Optical spectra obtained by heterodyning two integrated, unlocked widely tunable SG-DBR lasers.

Second, the FM tuning mechanism of the SG-DBR laser is very efficient. Unlike Distributed Feedback (DFB) lasers, which are tuned by current injection into the laser gain section, in SG-DBR lasers, the tuning is achieved by current injection into a small, separate, passive phase section. The DC FM sensitivity can be as high as 20 GHz/mA for this tuning mechanism, which is over an order of magnitude greater than the 1-3 GHz/mA DC FM sensitivity reported for a three-section laser optimized for use in OPLL applications [2]. The large FM sensitivity directly translates into a large feedback loop gain and thus helps improve OPLL stability.

Third, an important advantage of the SG-DBR laser is that, unlike in a typical DFB laser, there is no sign change in its FM phase response. The FM response has a 3dB bandwidth of ~70 MHz, and no phase inversion is observed below this frequency. The phase inversion in a DFB laser occurs within its bandwidth at a frequency where the thermal effect becomes too slow to dominate frequency tuning with the corresponding red shift in the FM response so that frequency tuning becomes dominated by the carrier-injection effect and the corresponding blue shift in the FM response. It is very challenging to implement an OPLL feedback electronic circuit that can compensate for this phase inversion. The absence of phase inversion in the FM phase response of an SG-DBR laser is due to the fact that a) the small and efficient phase tuning pads require small currents for tuning, thereby reducing the thermal effects, and b) the phase section is composed of the passive material that has a band gap larger than that of the active material so that the accumulation of carriers is very efficient as they cannot be depleted by stimulated emission.

Fourth, the linewidth of an SG-DBR laser is dominated by low-frequency jitter [39], which is not very difficult to compensate with the large bandwidth of an integrated OPLL, which as we will show below is at least 300 MHz.

We note that the Shawlow-Townes linewidth limit for a typical SG-DBR laser is typically below 1 MHz [39]. However, the linewidth that we measure with a 30-μs-delay self-homodyne technique is in the range 10 MHz to 50 MHz, varying with mirror setting, which is dominated by low-frequency jitter noise. This linewidth would be hard to compensate with an OPLL that is not integrated. Fig. 8 shows the combined linewidth from the heterodyne beat of two unlocked, integrated SG-DBR lasers by combining their outputs at an offset frequency. The combined linewidth of ~300 MHz is measured using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. This wide linewidth is associated with low frequency current noise on the tuning port, and this is normally removed with a large capacitive load in cases where rapid tuning is not required.

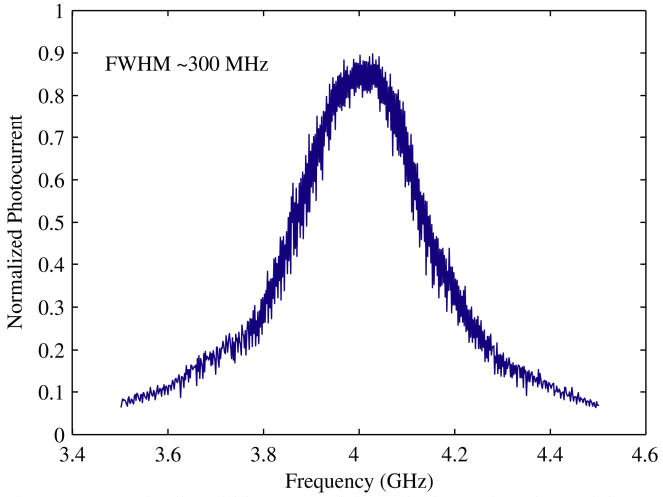


Fig. 8. Composite linewidth measured from the heterodyne beat of the two integrated, unlocked SG-DBR lasers. Resolution and video bandwidths are 2 MHz and 3 kHz, respectively.

IV. Proof-of-Concept Experimental Results

We perform two experiments in order to demonstrate proof-of-concept operation of the OPLL: homodyne locking and offset locking of the two monolithically integrated SG-DBR-lasers, as presented in subsections B and C below. Before presenting the details of these two experiments, we first present the basics of the electronics used in the feedback loop in subsection A.

A. Feedback Loop

Fig. 9 shows the schematic of OPLL-PIC including the feedback electronic circuit when used in the homodyne locking experiment, and Fig. 10 shows the corresponding optical image. The electronic circuit is built around a Field Effect Transistor (FET). One of the two photodetectors in the Middle Section of the OPLL-PIC is used to detect a phase error signal between the two lasers, which is converted to an amplitude

error signal in the 2x2 MMI. The reverse-biased current signal generated by this photodetector is amplified by the FET and converted into a forward-biased current signal needed to control the injection of carriers into the phase section of the slave SG-DBR laser.

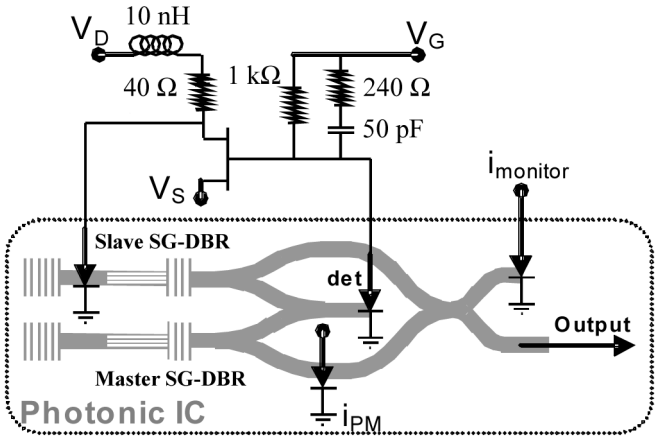


Fig. 9. Schematic of the homodyne locking experimental setup.

We design the detector load to provide a second order loop transfer function with lag compensation. The FM response of the SG-DBR laser has a 3-dB point around 70 MHz. The LR circuit that loads the laser phase section is designed to have a zero close to the laser's pole, compensating its FM response and making it a more controllable device. The RC circuit that loads the photodetector is designed to provide the following function. The larger of the two resistors dominates at frequencies closer to DC and ensures a large locking range. The other resistor dominates at frequencies closer to the 3-dB point and provides the desired zero needed to improve the stability of the loop for the higher frequencies where the gain becomes unity. The resulting loop bandwidth that we measure is ~300 MHz. Similar to a voltage-controlled oscillator an RF phase-locked loop, the laser itself acts as an integrator, which means that the rest of the electronics is required to provide a single pole to realize a second order loop. More details on the issues pertaining to the feedback loop design can be found in [40].

B. Homodyne Locking

As mentioned above, the schematic and optical image corresponding to the homodyne locking experiment are shown in Figs. 9 and 10, respectively. No current is applied to the back-side or the front-side mirror of the two SG-DBR lasers, so that they lase at their untuned wavelengths, which are close to 1542 nm. The random phase variation between the two lasers translates into an intensity modulated error signal at the output of the 2x2 MMI in the Middle Section of the OPLL-PIC and finally into a current error signal at the output of one of the photodetectors that is connected to the feedback loop. The error signal then passes through the electronic circuit and tunes the frequency of the slave laser so that it is matched to that of the master laser, where the slave laser effectively plays a role of a current-controlled oscillator.

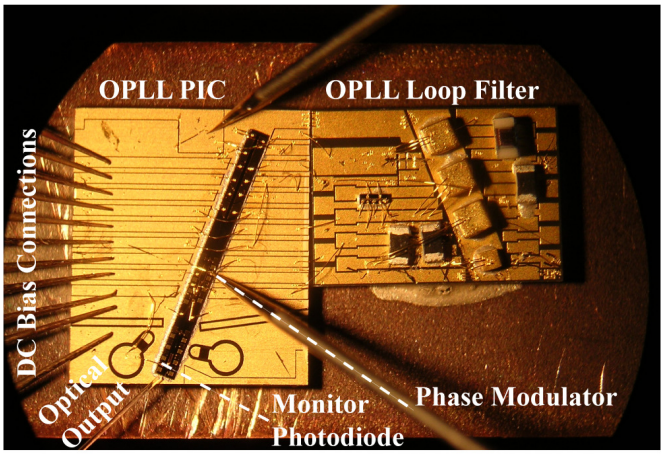


Fig. 10. Optical image of the homodyne locking experimental setup.

In order to bring the OPLL from an unlocked state into a locked state, we inject appropriate bias currents into the phase section of the one of the SG-DBR laser until its frequency is within the feedback loop bandwidth, i.e. ~300 MHz, to that of the second SG-DBR laser. The bias current is adjusted until the noise spectrum measured at the optical output of the OPLL-PIC changes as shown in Fig. 11, which indicates that the OPLL-PIC has fallen into a locked state. Fig. 11 also reveals the expected presence of the 300 MHz resonance frequency peak, above which the OPLL provides a positive rather than negative feedback and becomes unstable. The data is acquired using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. The uncompensated low-frequency noise below the resonance frequency peak is mainly due to OPLL-PIC's AM noise that can be effectively cancelled using feedback from a balanced photodetector pair (implemented on the PIC, but not used here) rather than a single photodetector.

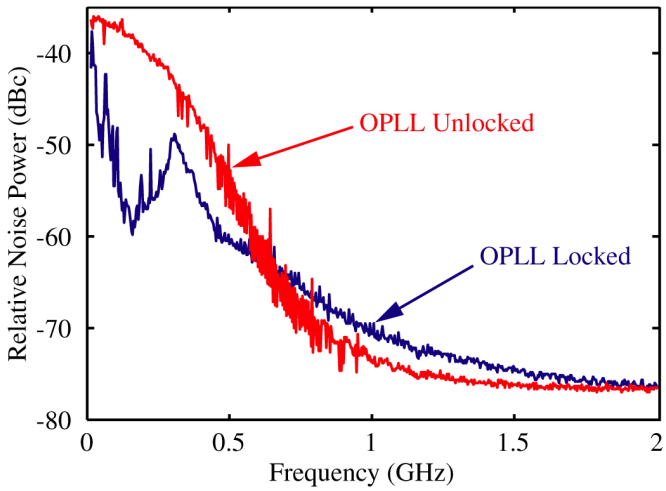


Fig. 11. Noise spectra measured at the optical output of the OPLL-PIC in the homodyne locking experiment. Resolution and video bandwidths are 2 MHz and 10 kHz, respectively.

To further confirm the homodyne locking, we inject current into one of the modulators and continuously adjust the phase

of the light from one of the SG-DBR lasers. This modulator is part of the waveguide that directs light toward the 2x2 MMI in the Output Section of the OPLL-PIC and is not the feedback-loop. This phase modulator allows us to independently modulate the phase of one SG-DBR laser output while leaving the phase of the second SG-DBR laser unchanged. When the OPLL is in the locked state, the two lasers are coherent with respect to each other. By changing the phase on one of the lasers, the interference between the two lasers in the 2x2 MMI in the Output Section of the OPLL-PIC shows the characteristic interference that is observed from a Mach-Zehnder Interferometer (MZI), which converts phase modulation to amplitude modulation. When the OPLL is not locked, the two lasers are not coherent with respect to each other and their interference in the 2x2 MMI does not exhibit the phase to amplitude modulation response that is characteristic of an MZI.

Fig. 12 illustrates this behavior for both locked and unlocked states of the OPLL. In both cases, we see a small intensity modulation characteristic for our modulators when operated in the forward bias. Also, the half-wave current (I_π) needed for switching the interference between "on" and "off" states is ~4 mA, which is consistent with other measurements performed on similar phase modulators. The extinction ratio (~8 dB) observed for the constructive versus destructive interference is limited by unequal optical powers reaching the 2x2 MMI, phase noise of the lasers, weak multimoding in the waveguides, and polarization mismatch. Because the SG-DBR lasers emit quasi-TE-polarized light and all of the integrated optical components are design to be polarization maintaining, the polarization mismatch is expected to have a small effect on the extinction ratio. Due to the present probing station limitations *i.e.*, limited number of bias controls, in this proof-of-concept study, we did not bias the SOAs independently nor did we tune the MMI splitters in order to overcome the possible optical power mismatch. This issue will be addressed more systematically in a future study.

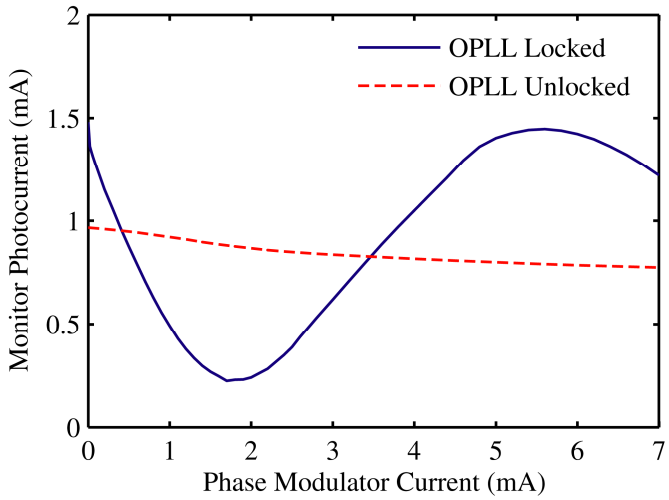


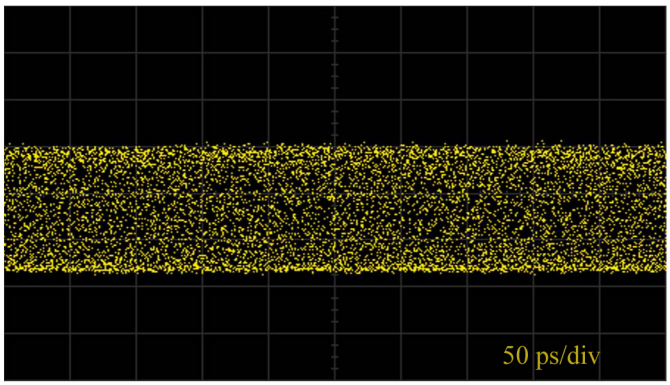
Fig. 12. Phase-to-amplitude modulation conversion observed for the locked and unlocked states of the OPLL for homodyne locking of the two SG-DBR lasers.

C. *Offset Locking*

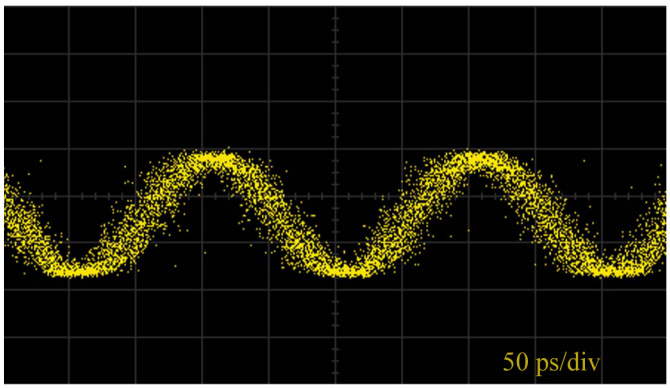
The same PIC and electronic circuit that were used in the homodyne experiment are also used in the offset locking experiment. To demonstrate offset-locking of the two monolithically integrated SG-DBR lasers, we apply a reverse bias phase modulation to one of the modulators that is connected to the output of the 2x2 MMI in the Middle Section of the OPLL-PIC and is a part of the feedback loop, as shown in Fig 1. As this phase modulator output is only connected to the integrated detector pair used for the feedback circuit, the OPLL-PIC output signal does not contain any modulation sidebands. In this case, we use the reverse bias amplitude modulation based on the Franz-Keldysh effect because the GHz-range modulation frequency that we need far exceeds the bandwidth (~100 MHz) of the modulator in the forward-biased current-injection mode. In our offset-locking scheme, the carrier frequencies from both lasers are simultaneously modulated, which generates two modulation sidebands corresponding to either laser's carrier frequency. When the frequency separation between the two SG-DBR lasers equals the modulation frequency, the detected photocurrent will contain a phase-dependent DC component, and sideband locking of the two lasers becomes possible. Mixing of the two laser frequencies and their sidebands occurs in the photodetector, which generates a corresponding current error signal to the feedback electronics and the phase section of the slave laser whenever there is a random phase walk-off between a center frequency of one laser and a sideband of the other laser. The power in the sidebands is smaller in comparison to the power at the center frequencies of the laser. Consequently, the extinction ratio of the corresponding interference is smaller than for the homodyne OPLL, producing a weaker error signal. To compensate for this, to generate as strong modulation sidebands as possible, the power applied to the modulator used in offset locking is between 10 dBm and 15 dBm.

Figs. 13(a) and 13(b) show an oscilloscope trace of the OPLL-PIC's optical output before and after 5 GHz offset locking of the two SG-DBR lasers, respectively. The oscilloscope is triggered by the 5 GHz modulating signal. Before locking, the phase of the beat varies randomly and only an envelope of the beat is observed in Fig. 13 (a). After phase-locking, a coherent beat signal is generated, as observed by the oscilloscope trace in Fig. 13(b).

In addition to the time domain representation of the locked beat shown in Fig 13 (b), in Fig. 14, we plot the corresponding frequency spectrum obtained using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. As expected, the spectrum is centered at the 5 GHz modulation frequency, surrounded by two peaks that are offset by ~300 MHz, corresponding to the bandwidth of the feedback loop. From the spectrum in Fig. 14, we calculated the phase error variance to be 0.03 rad^2 by dividing the noise power within the 2 GHz span by the signal power [3]. Our result is comparable to the state-of-the-art result in [2], where phase error radiance of 0.05 rad^2 in a 1 GHz bandwidth has been reported for an



(a)



(b)

Fig. 13. Oscilloscope traces observed at the optical output of the OPLL-PIC in the heterodyne locking experiment when the OPLL is (a) unlocked and (b) locked.

OPLL based on miniature bulk optics is designed for use in a microwave photonic transmitter. We obtained similar results for different offset frequencies up to 15 GHz.

V. Conclusion

In this work, we have successfully demonstrated the first monolithically integrated optical phase-locked loop photonic integrated circuit in which all of the optical components are integrated on the same InP platform, including: master and slave SG-DBR lasers, high-speed modulators, high-speed photo detectors, multimode interference couples/splitters, as well as interconnecting optical waveguides. Compared to the alternatives, monolithic integration an optical phase-locked loop is expected not only to provide a competitive performance, but also to make the technology more easily packaged and less expensive.

We have shown that, via monolithic integration, the phase-locked loop can be made sufficiently compact, and thus have a sufficiently wide bandwidth (300 MHz), to allow use of wide linewidth semiconductor lasers. We have further demonstrated suitability of SG-DBR lasers to be used as the master laser and the slave laser, *i.e.*, current-controlled oscillator, in this application. Most importantly, unlike the DFB laser, the slave SG-DBR laser does not suffer from a phase inversion in the FM frequency response, which is not easily compensated by the loop filter electronics. In addition, the slave SG-DBR laser offers a large phase tuning sensitivity, improving the gain and stability of the phase-locked loop. We have also shown that the detuning range of the master and slave SG-DBR lasers exceeds 5 THz, which enables the phase-locked loop to generate phase-stable optical beats at very high frequencies. This beat can be modulated with on-chip high-speed modulators and also converted into an electrical signal with on-chip high-speed photodetectors.

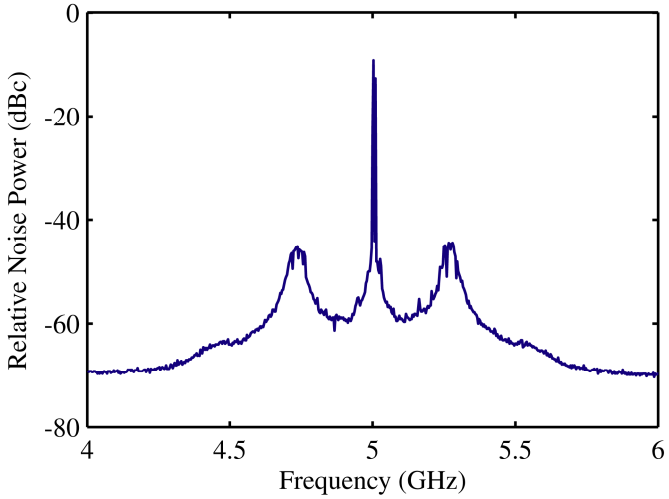


Fig. 14. Noise spectrum measured at the optical output of the OPLL-PIC in the heterodyne locking experiment. Resolution and video bandwidths are 2 MHz and 10 kHz, respectively.

We have performed two experiments to demonstrate the proof-of-concept operation of the monolithically integrated phase-locked loop: homodyne locking and offset (5 GHz offset) locking of the master and slave SG-DBR lasers. We have shown that a simple electronic filter is sufficient to enable locking. The future versions of optical phased-locked loop will utilize both feedback photodetectors as a balanced pair in order to reduce laser amplitude noise. In addition, integrated feedback electronics will be implemented to further increase the bandwidth of the loop. Both of the changes are expected to significantly reduce the phase noise of the phase-locked loop.

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

Acknowledgment

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